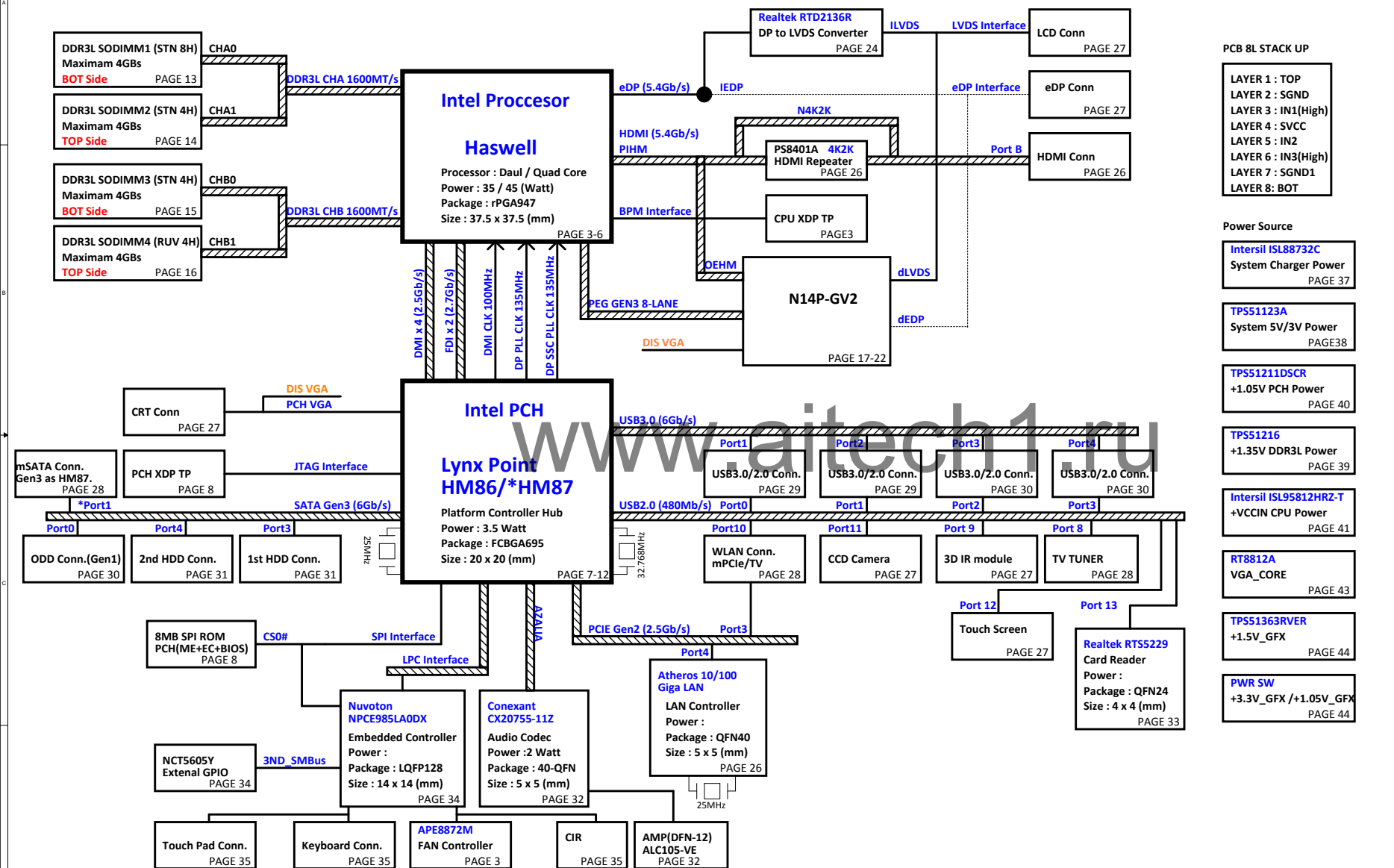
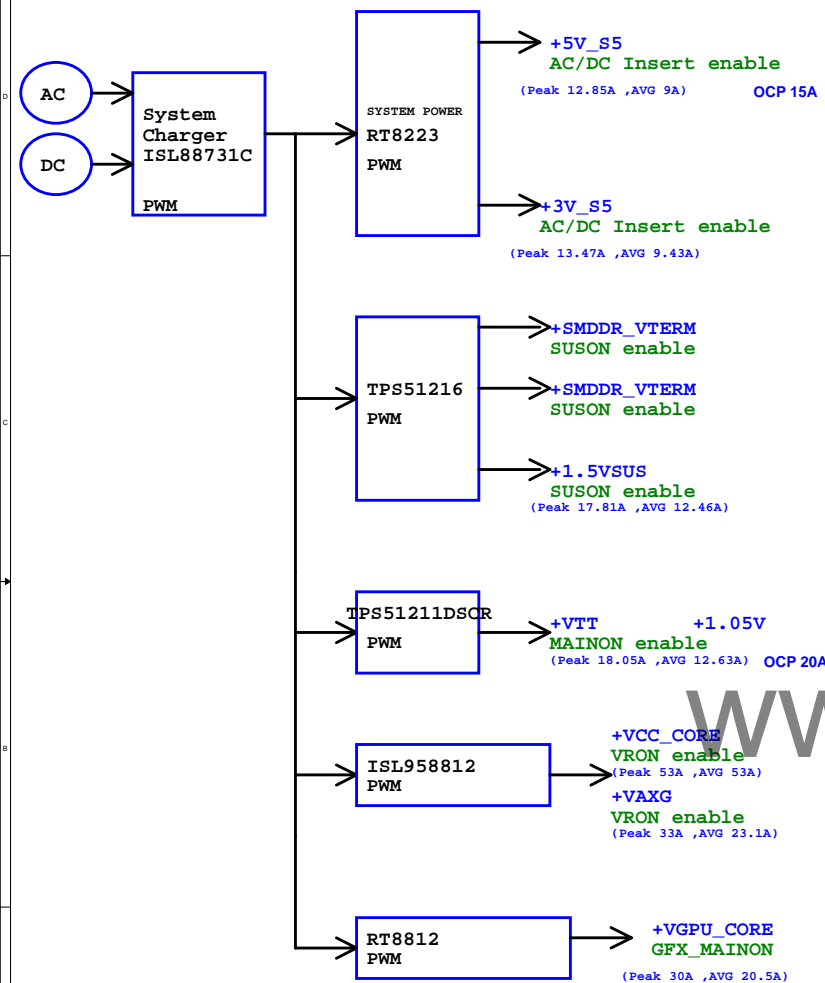


(17.3") Intel Shark Bay Platform Block Diagram

01



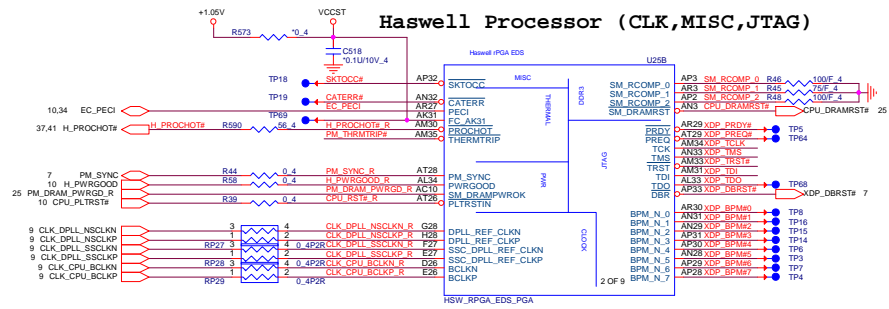


POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

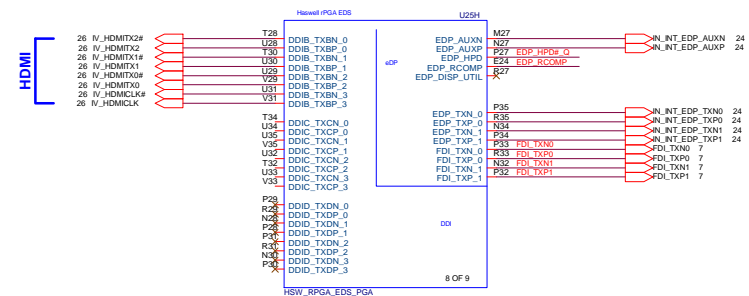
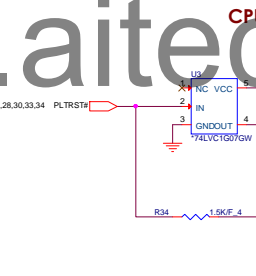
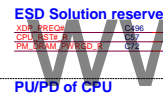
Haswell Processor (DMI,PEG,FDI)



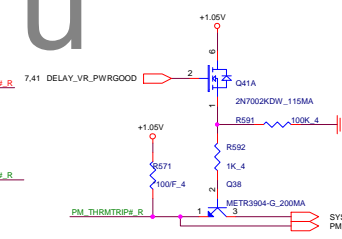
Haswell Processor (CLK,MISC,JTAG)



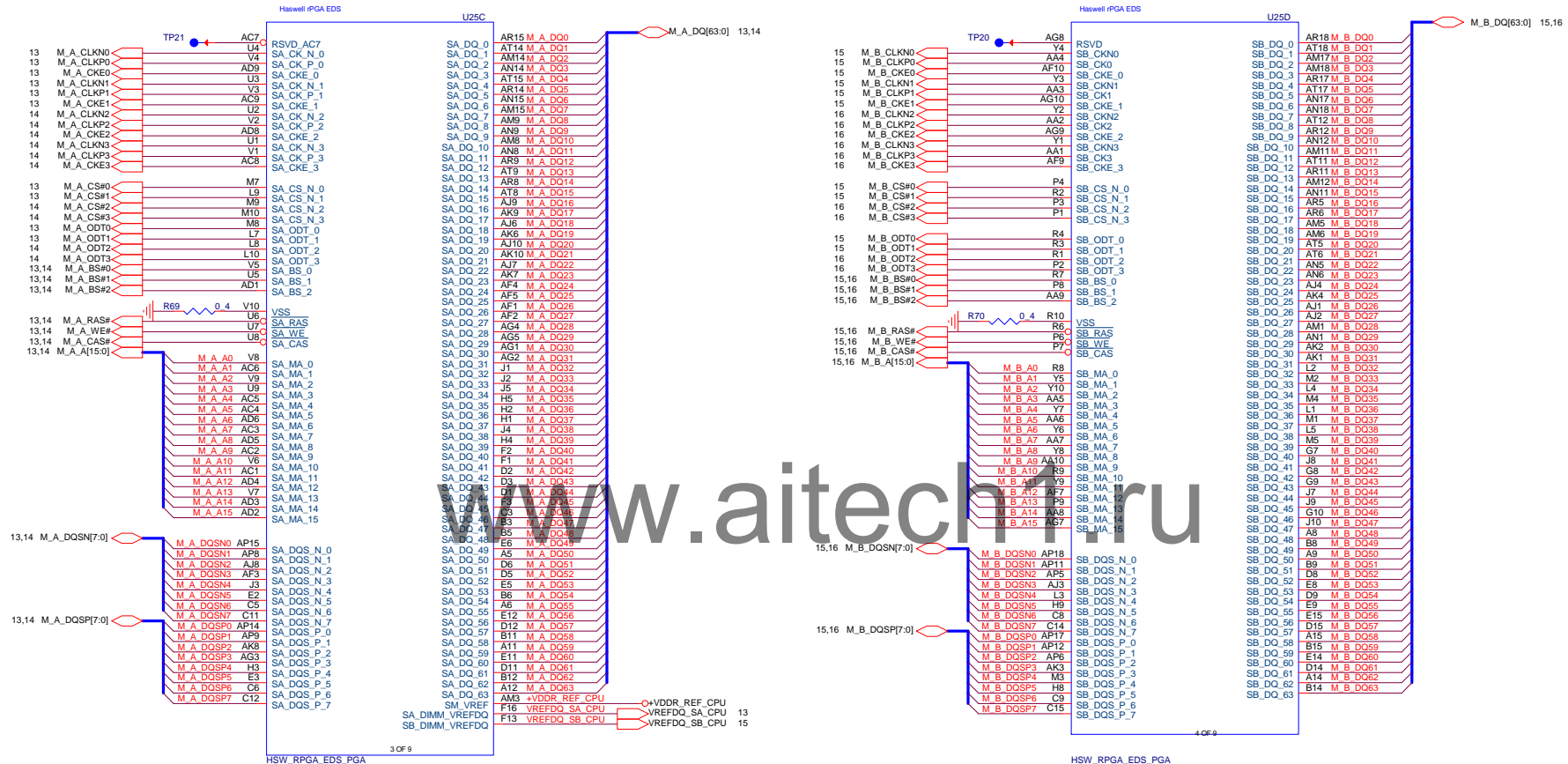
Haswell Processor (DDI,eDP,FDI)

FDI Disabling (Discrete Only)
<CPU>DP & PEG Compensation
<CPU>

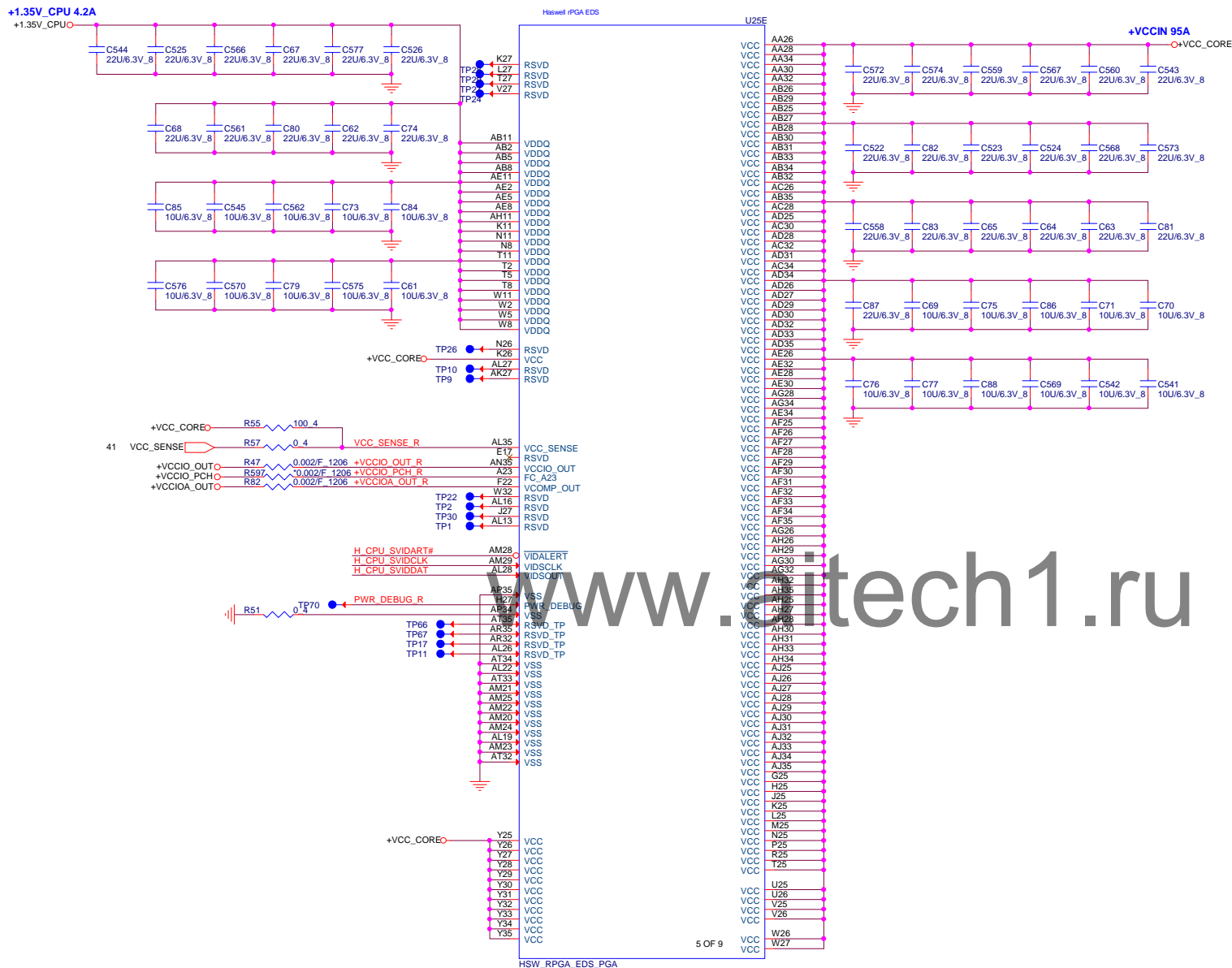
Thermal Trip & Process HOT CPU



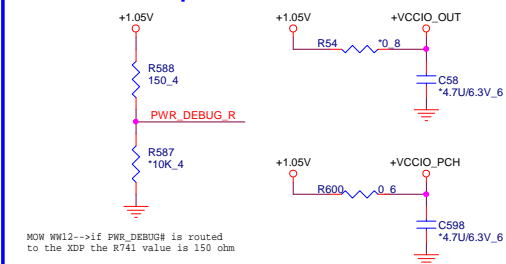
Haswell Processor (DDR3)



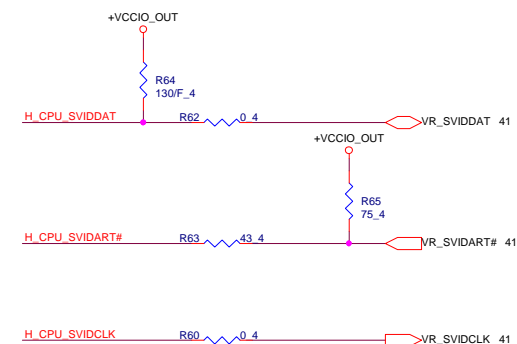
Haswell Processor (POWER)



Power Test Propose



SVID

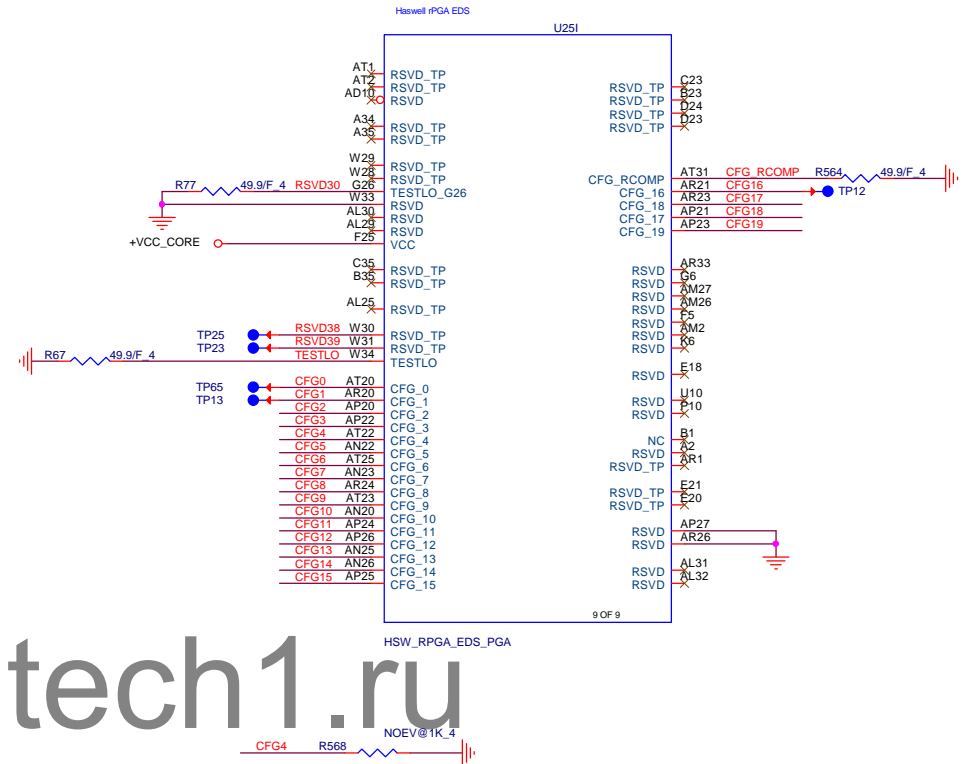
**Quanta Computer Inc.**

PROJECT : BDBD

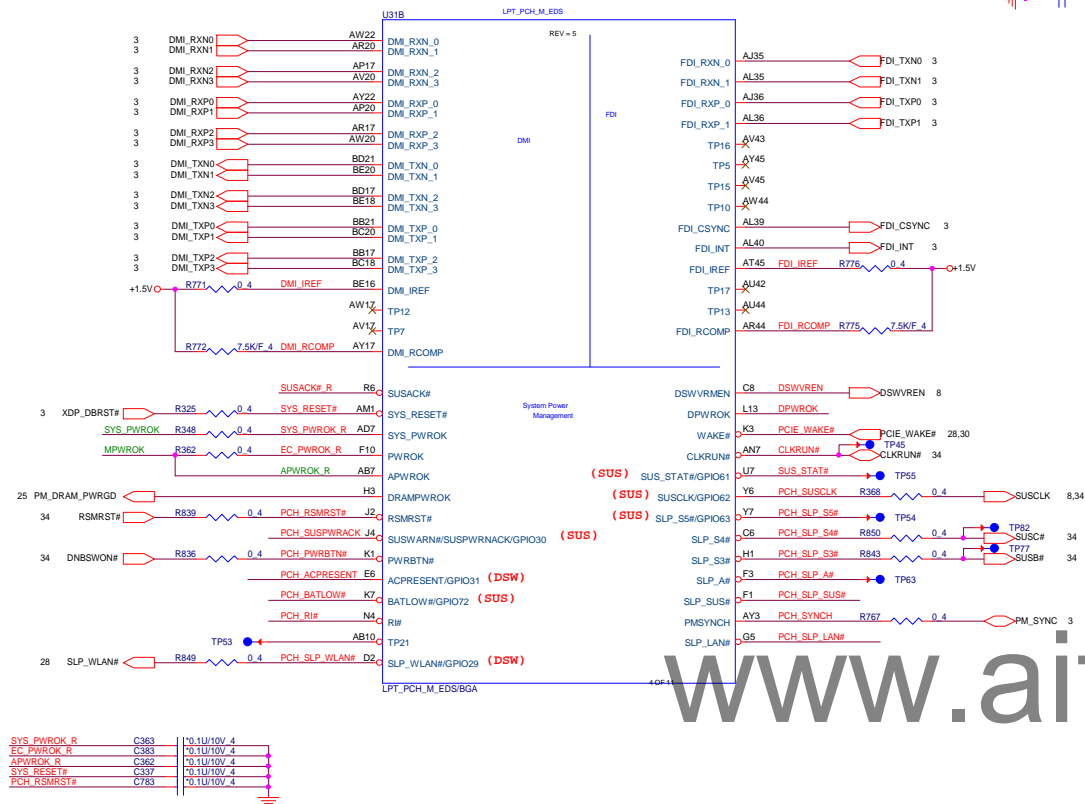
Size	Document Number Haswell 4/5 (POWER)	Rev 2A
Date:	Monday, December 17, 2012	Sheet 5 of 45

Date: Monday, December 17, 2012 Sheet 5 of 45

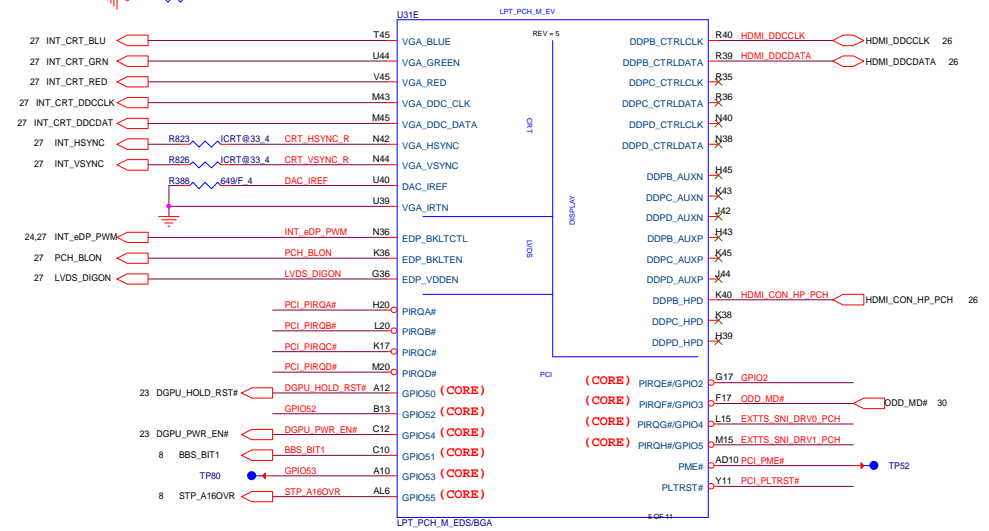
Date: Monday, December 17, 2012 Sheet 5 of 45



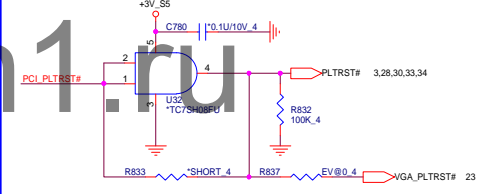
Lynx Point (DMI,FDI,PM)



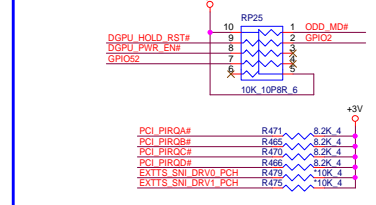
Lynx Point (CRT,PCI,DDI CNTL)



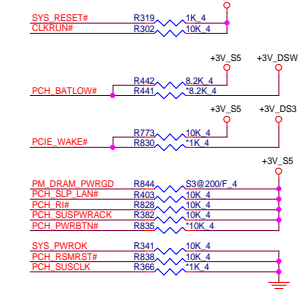
PLTRST# Buffer



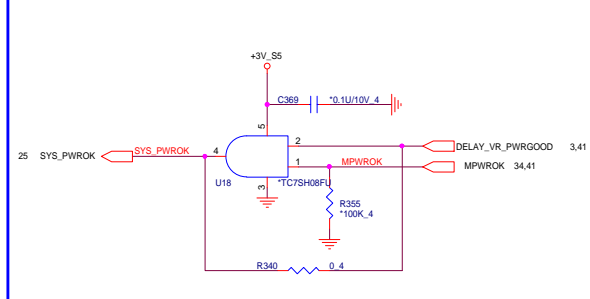
PCI PU



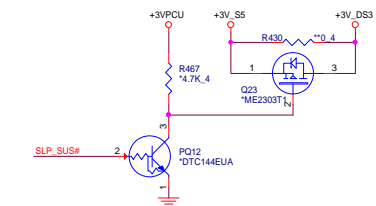
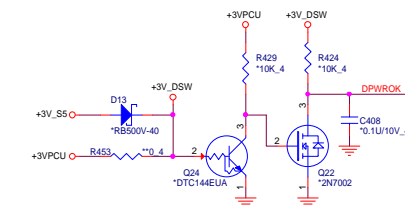
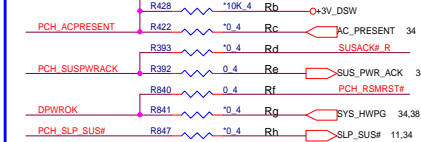
PCH PM PU/PD



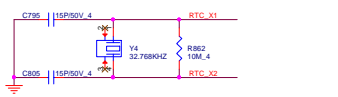
SYSPWOK



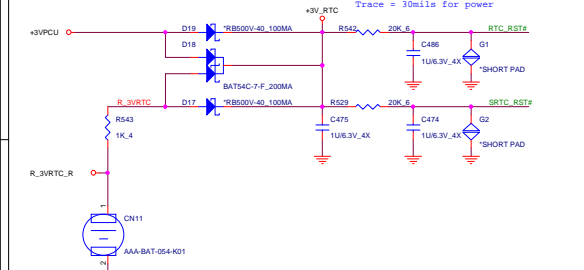
DSW Circuit



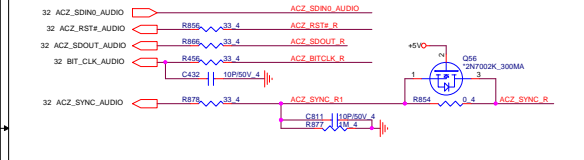
RTC Clock 32.768KHz (RTC)



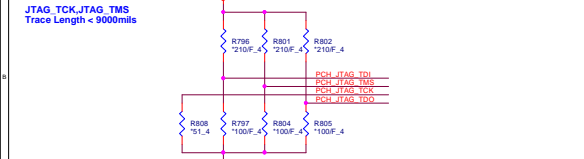
RTC Circuitry (RTC)



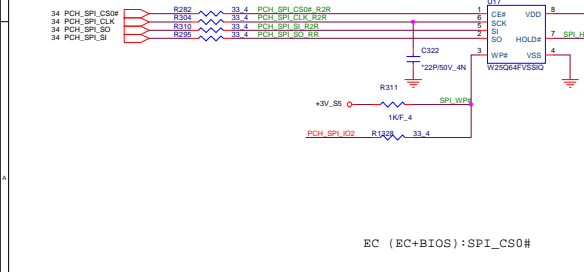
HDA



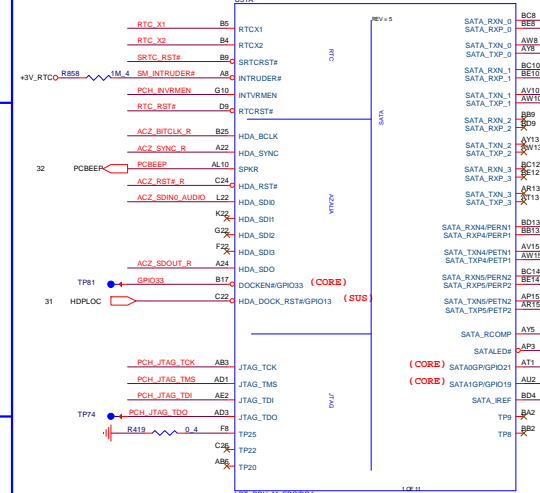
PCH JTAG



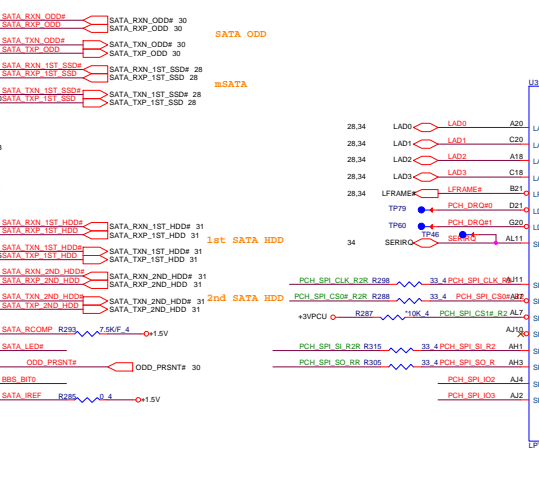
PCH Dual SPI CLG



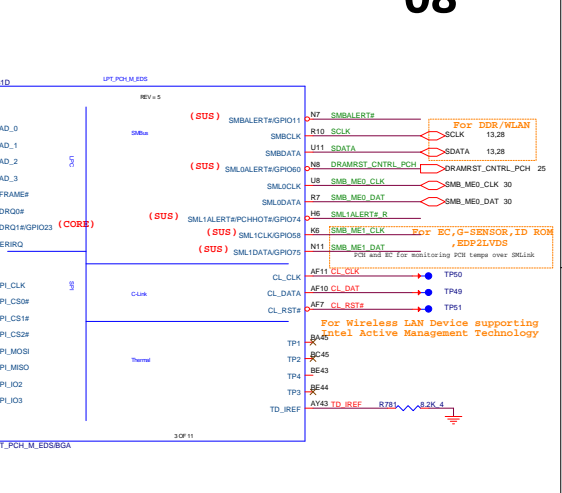
Lynx Point (RTC,IHDA,SATA,JTAG)



Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)



08



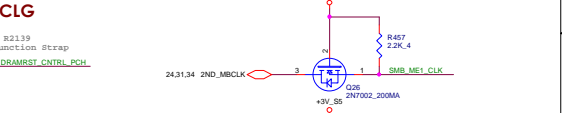
CLG



SMBus/Pull-up CLG

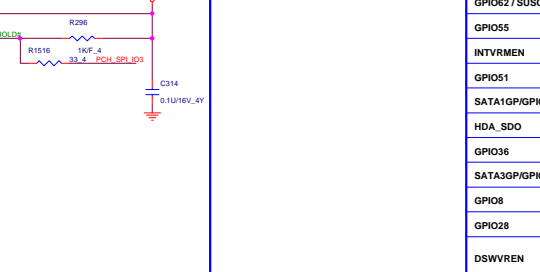


CLG

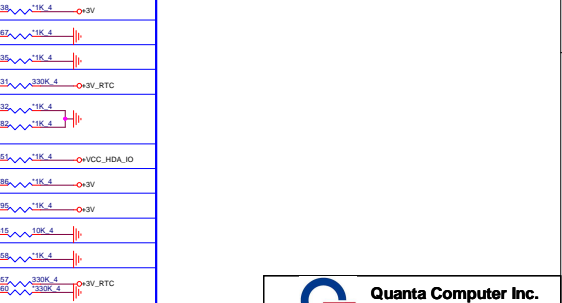


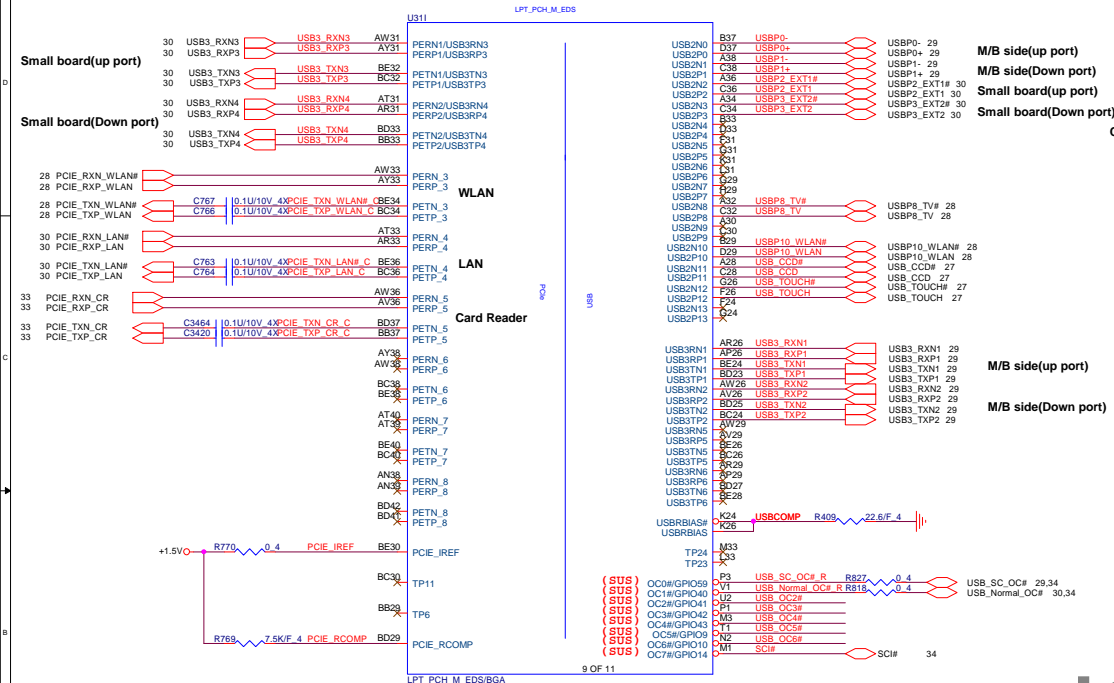
www.aitech1.ru

PCH STRAPPING

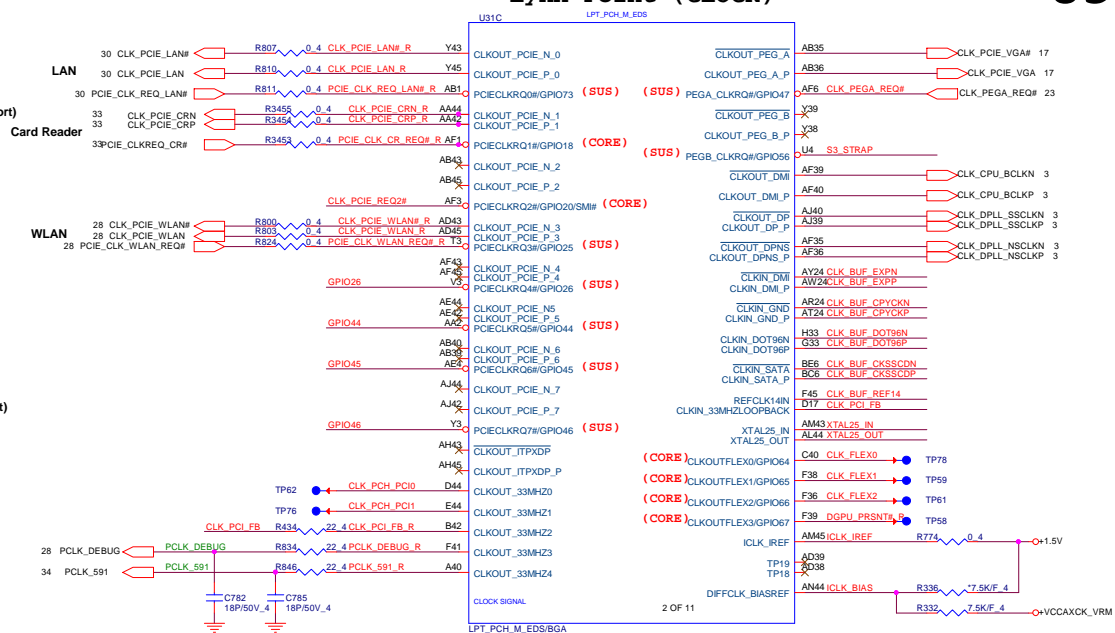


Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	PCBEEP R438 *1K_4 -> +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	7,34 SUSCLK R387 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Disable 1 = Top-Block Swap mode 1 = Default (Int PU)	7 STP_A16OVH R338 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH INVRMEN R311 *330K_4 -> +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	B01 Bit 0 1 0 Reserved 1 1 SPI 0 0 LPC	7 BBS_BIT1 R432 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		BBS_BIT0 R792 *1K_4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	34 ACZ_SDOOUT R885 *1K_4 -> VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	10 GPIO36 R786 *1K_4 -> +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	10 FDI_OVRVLTO R795 *1K_4 -> +3V
GPIO8	RSVD	RSMRST#	Internal PU	10 GPIO8 R818 *10K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	0 PLL_ODVR_EN R358 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	DSWVREN R881 *330K_4 -> +3V_RTC



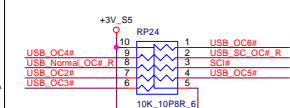


Lynx Point (CLOCK)

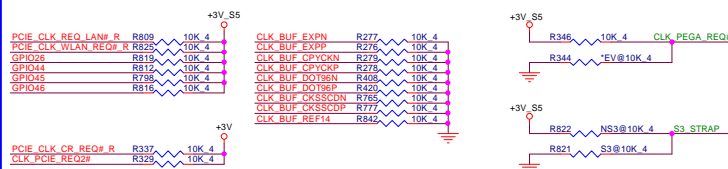


www.aitech1.ru

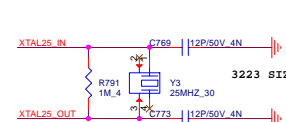
USB Overcurrent

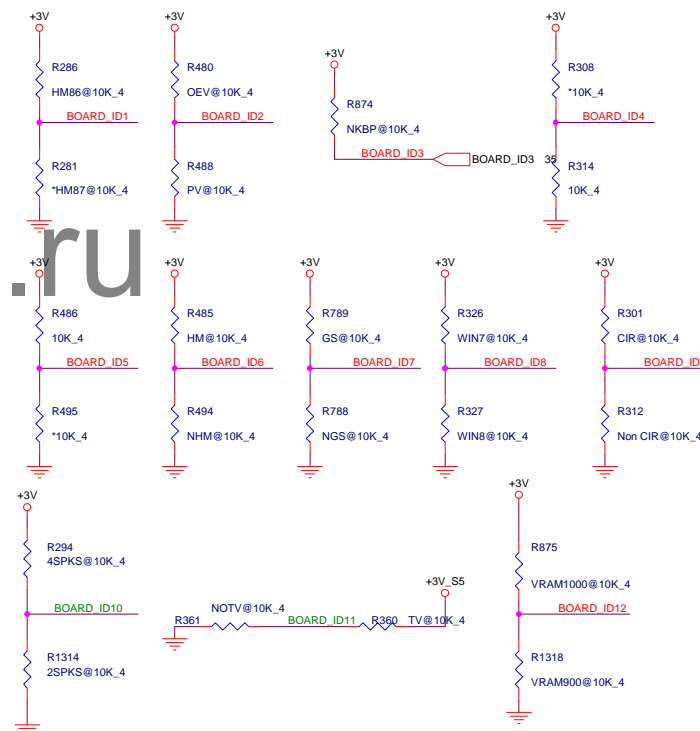


PCH Internal Clock

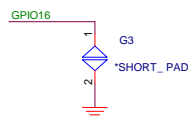


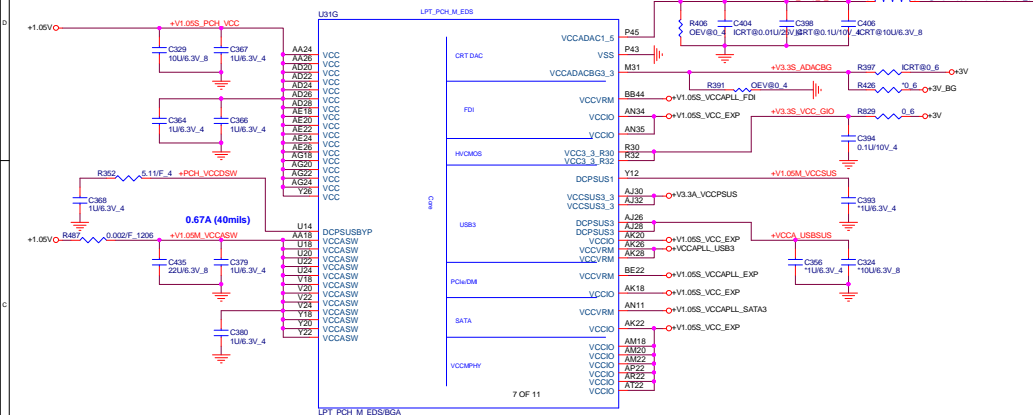
25MHz Crystal for PCH



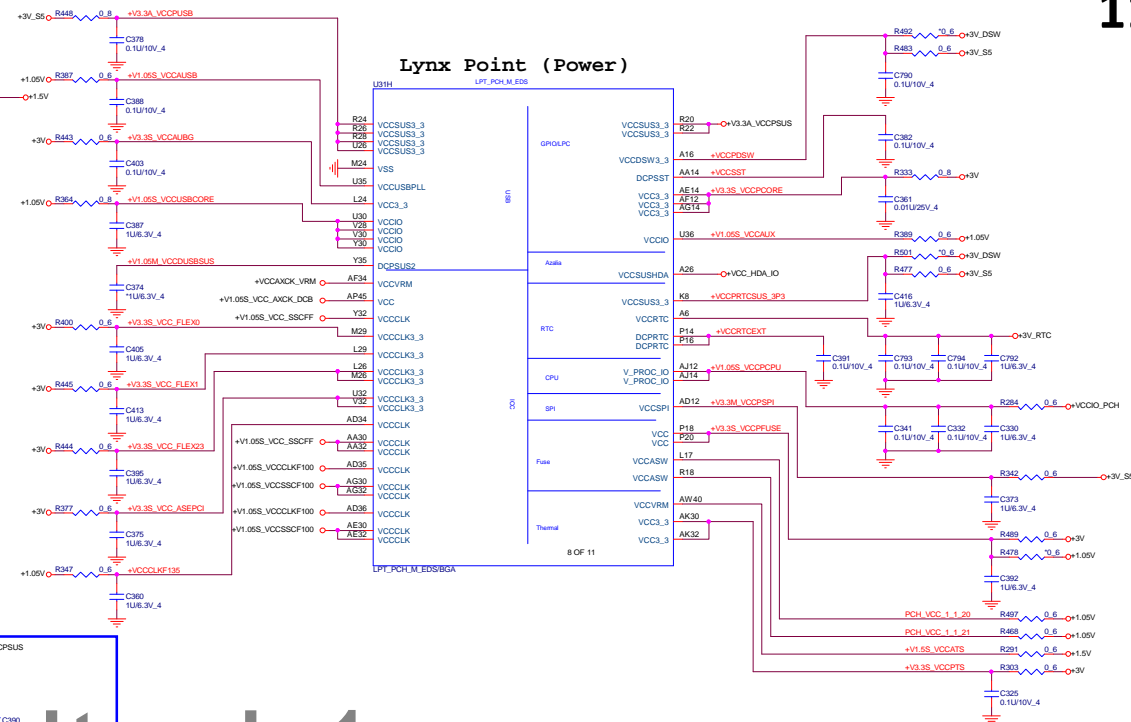


PCH MISC PU/PD

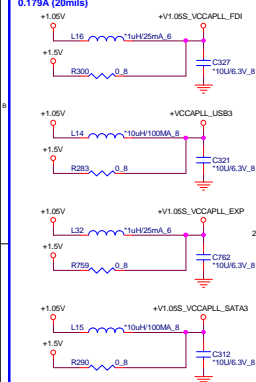




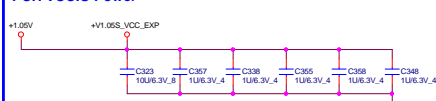
Lynx Point (Power)



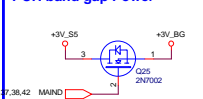
PCH VRM Power
0.179A (20mils)



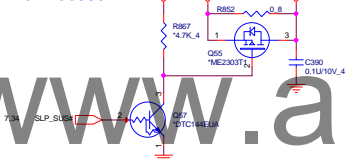
PCH VCCIO Power



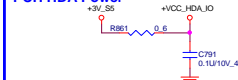
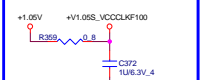
PCH band gap Power

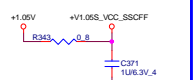


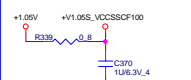
PCH VCCSUS



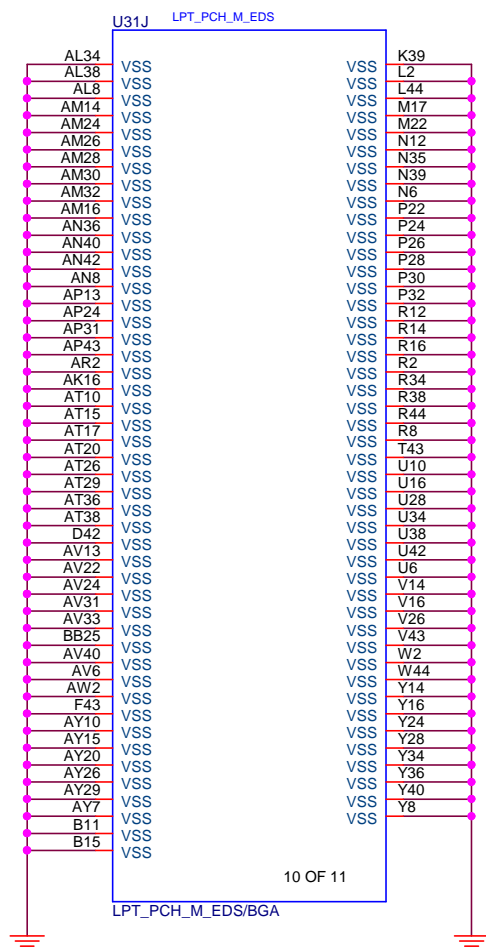
PCH HDA Power	0.0
---------------	-----

[illegible]

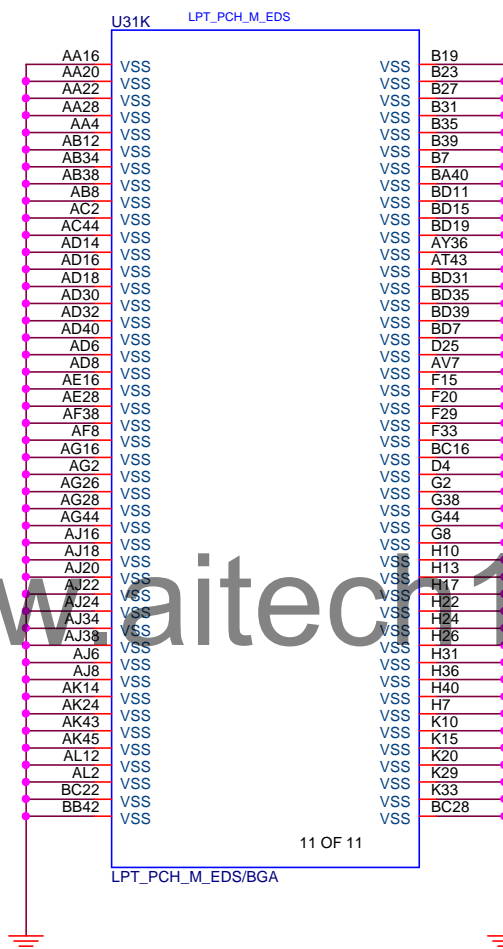




Lynx Point (GND)



Lynx Point (GND)

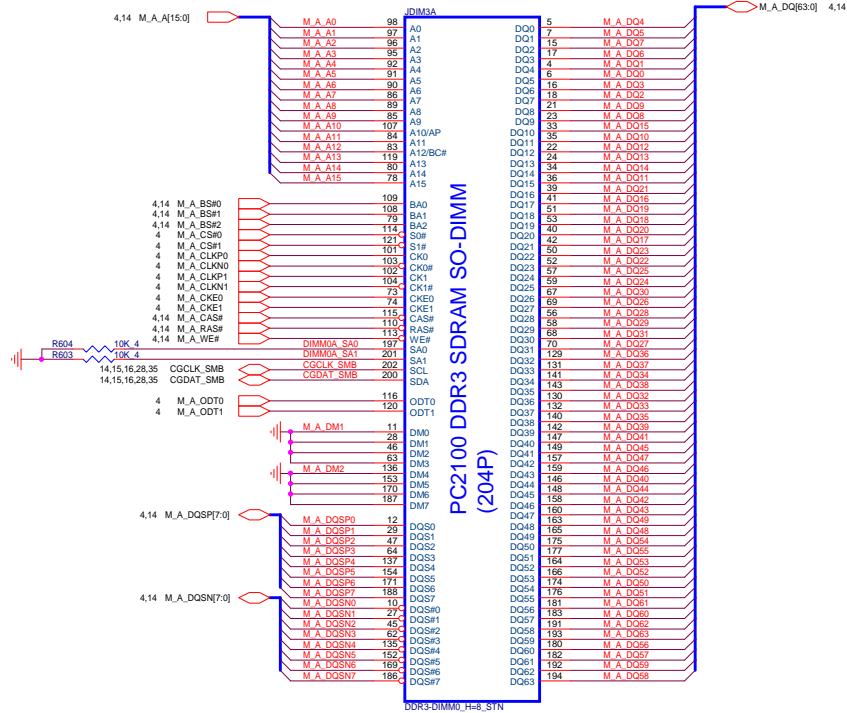


Quanta Computer Inc.

PROJECT : BDBD

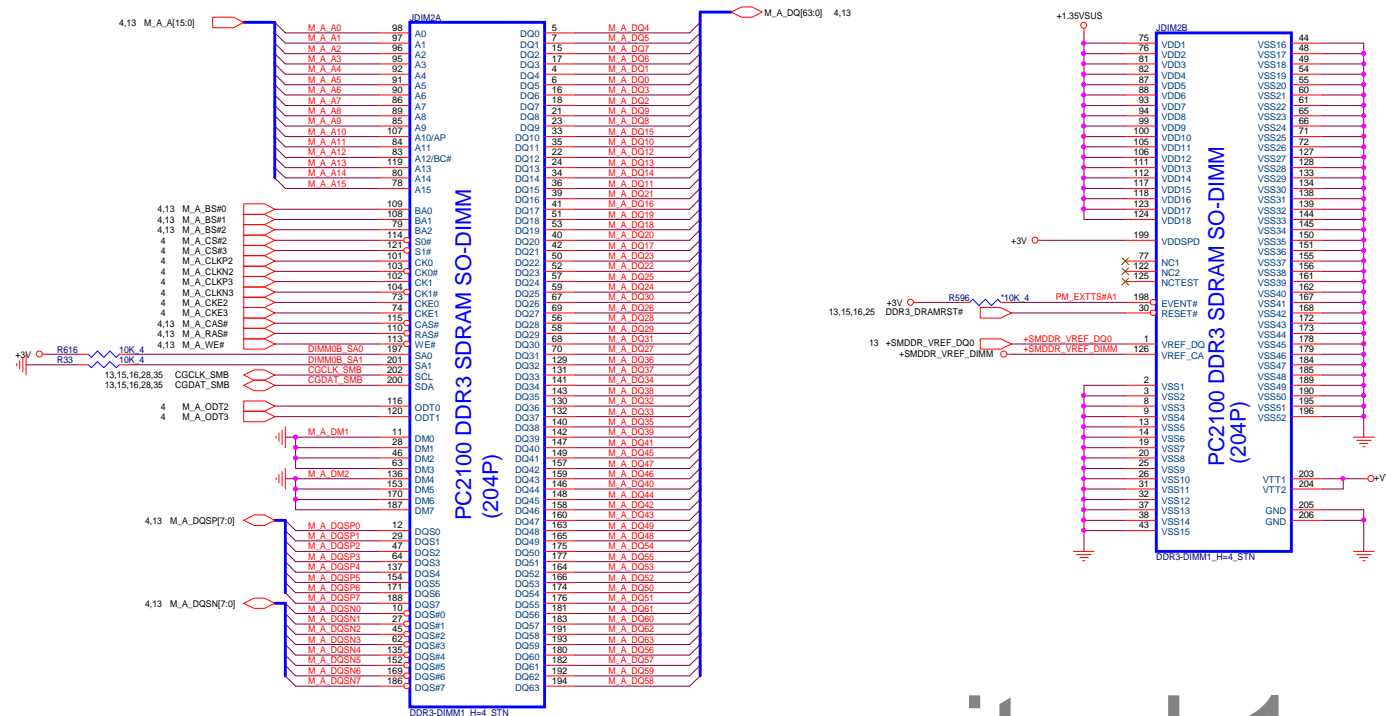
Size	Document Number	Rev
	LPT 6/6 (GND)	2A
Date:	Monday, December 17, 2012	Sheet 12 of 45

BOT side Close to CPU

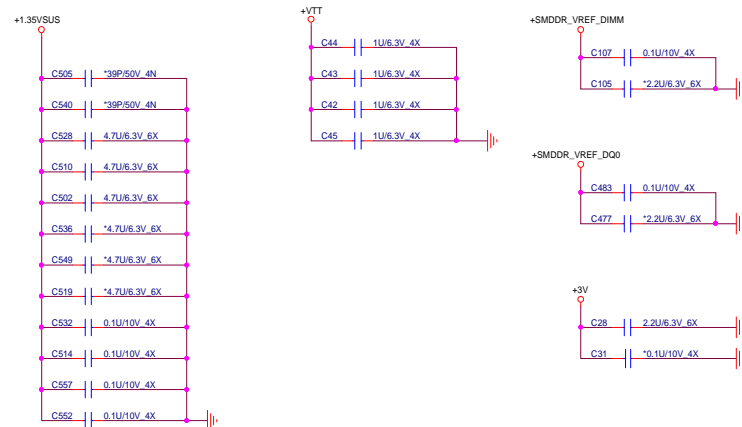


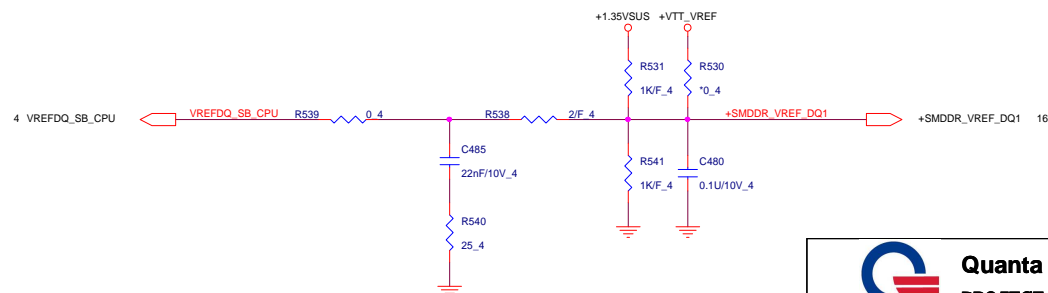
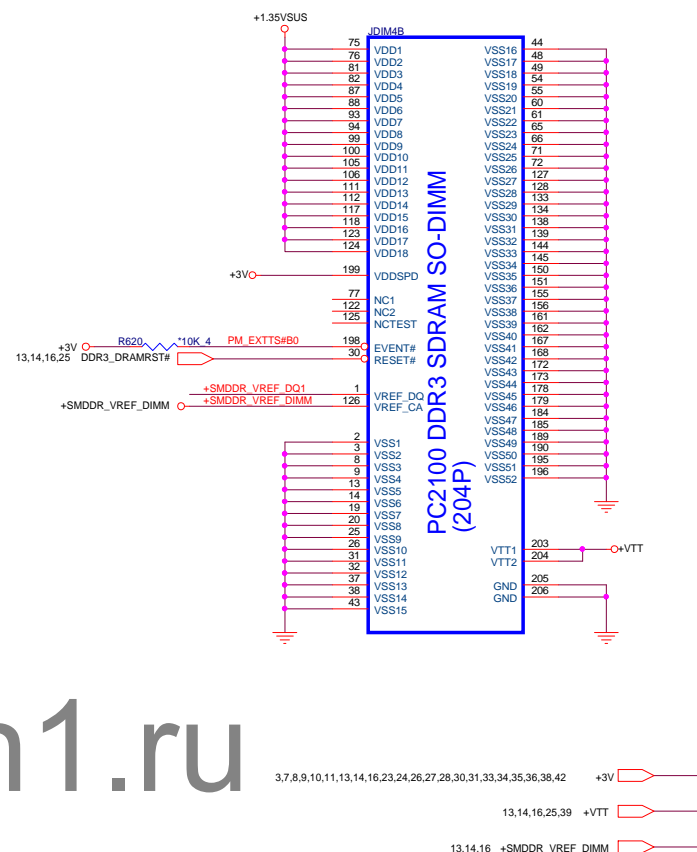
TOP side Close to CPU

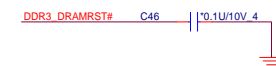
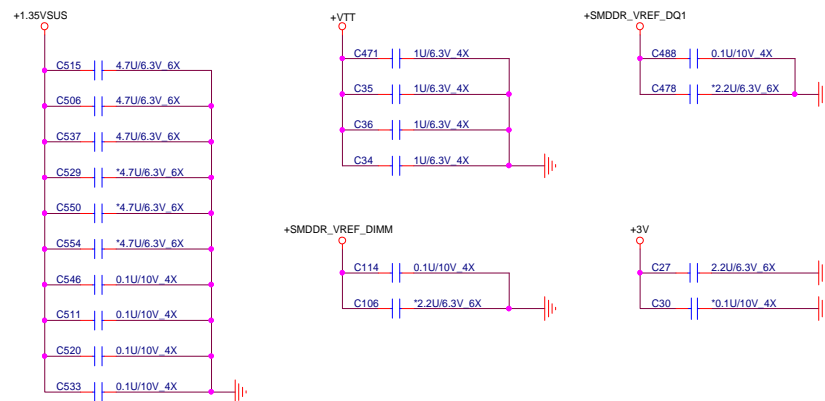
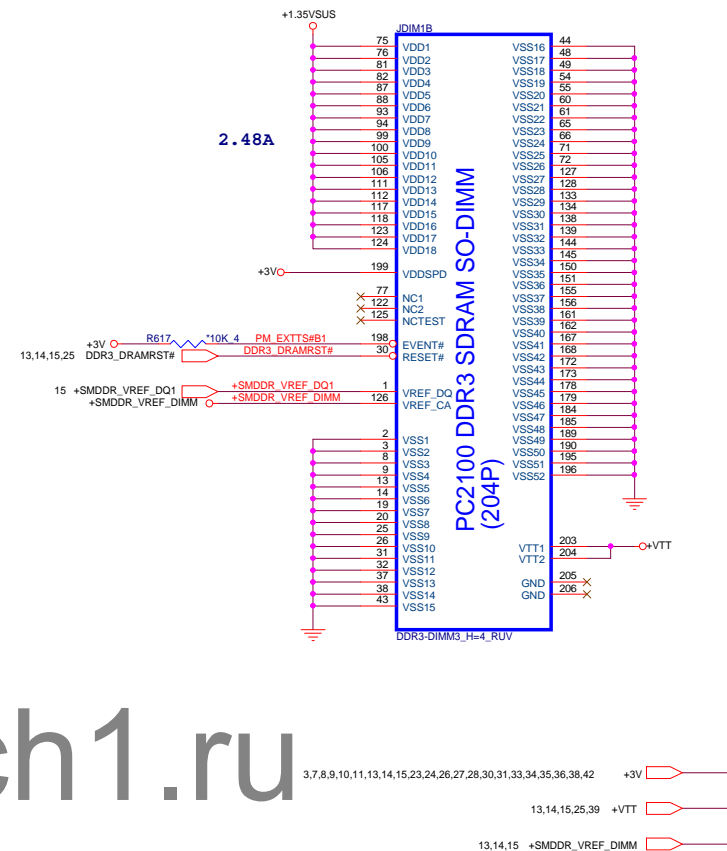
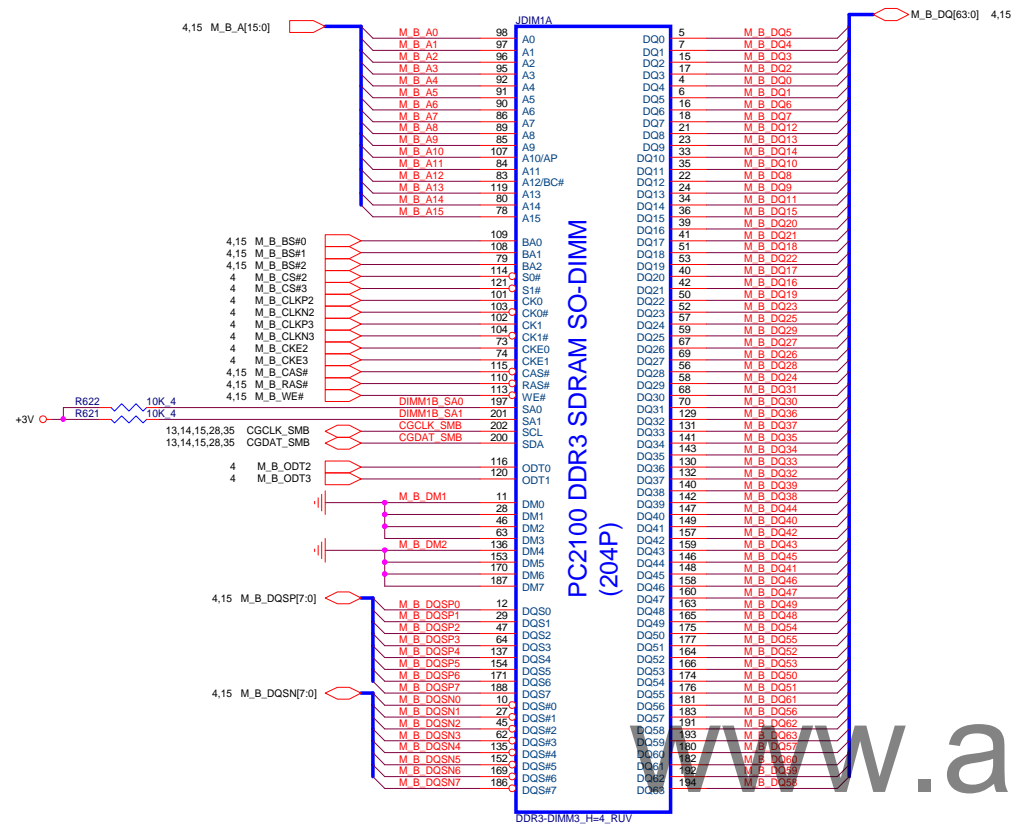
14

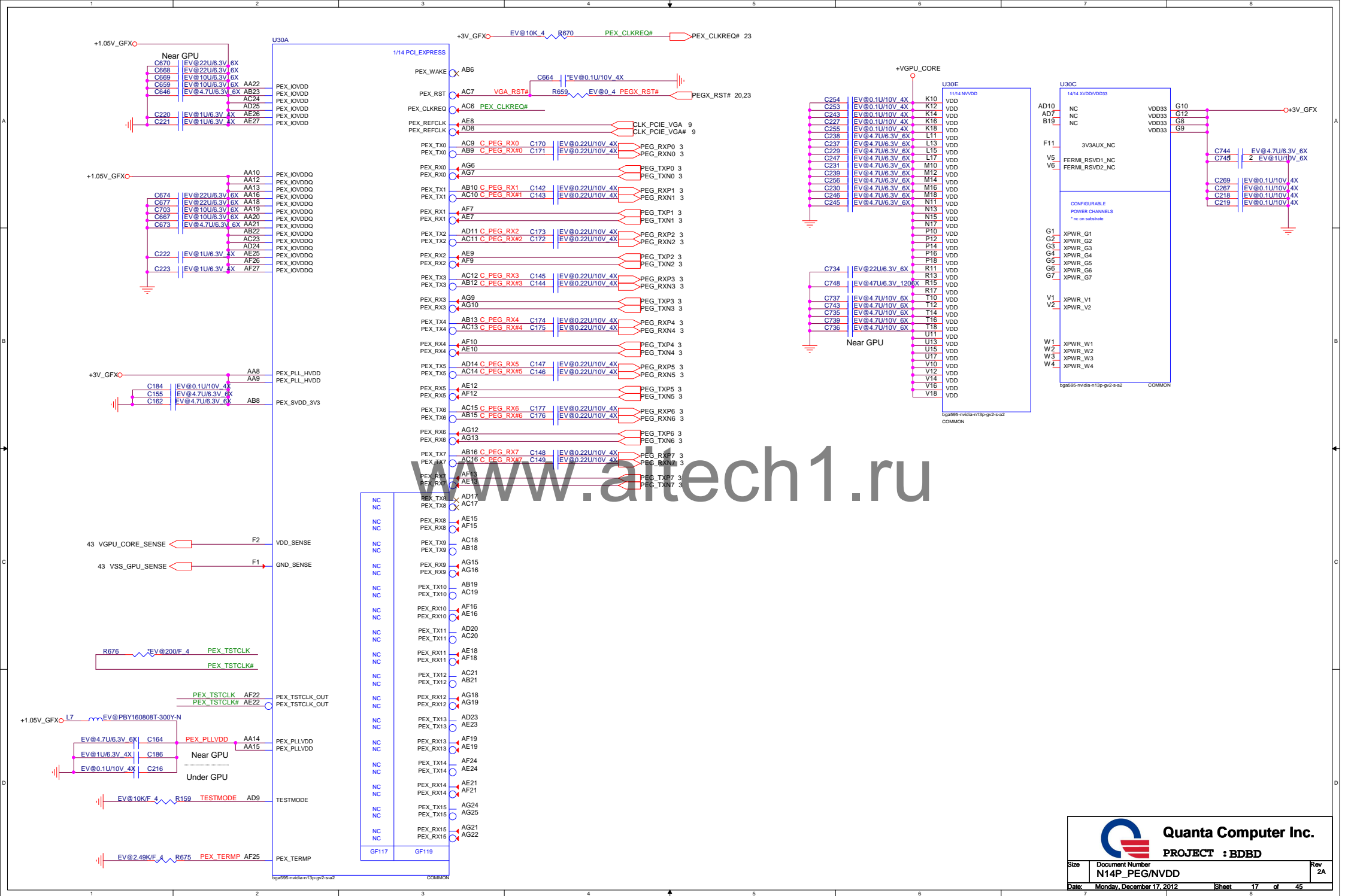


www.aitech1.ru



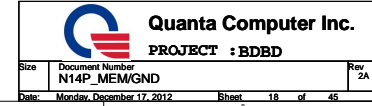


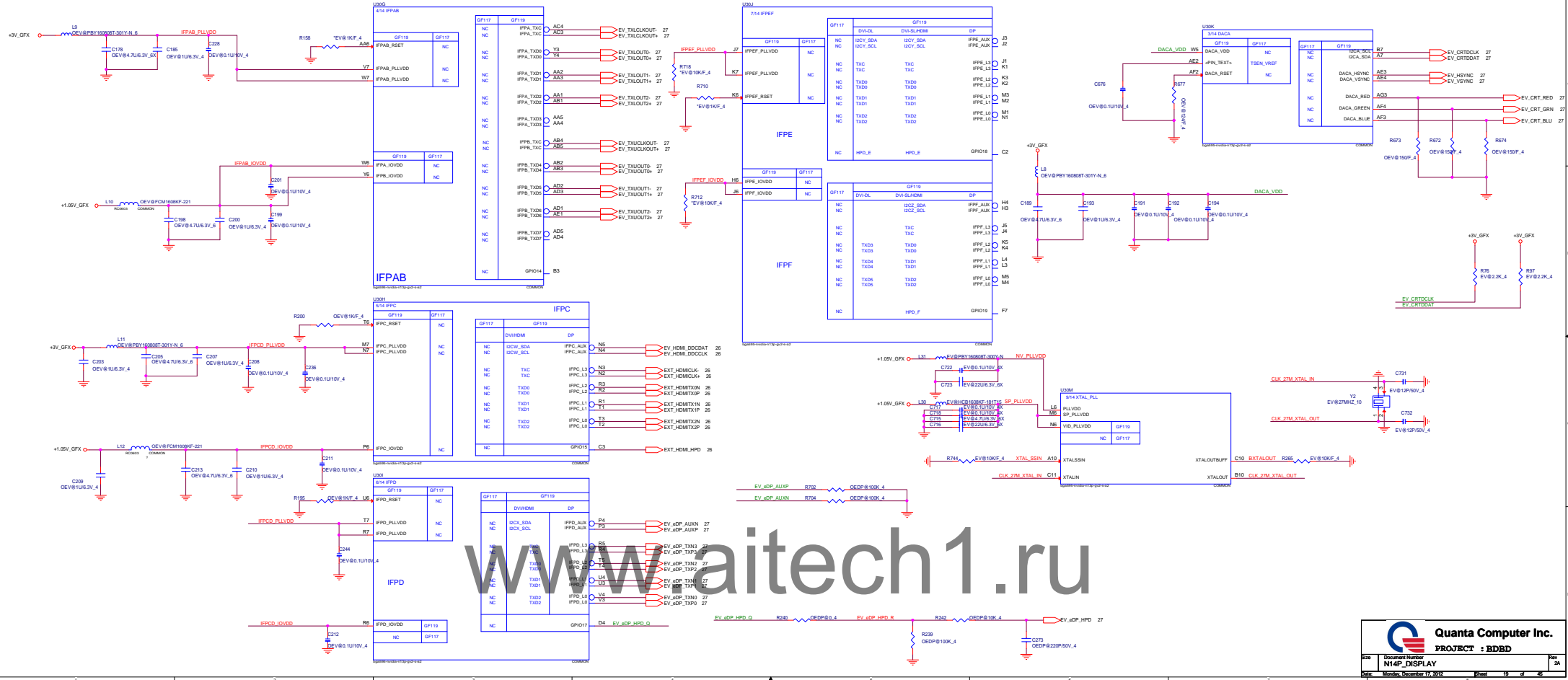


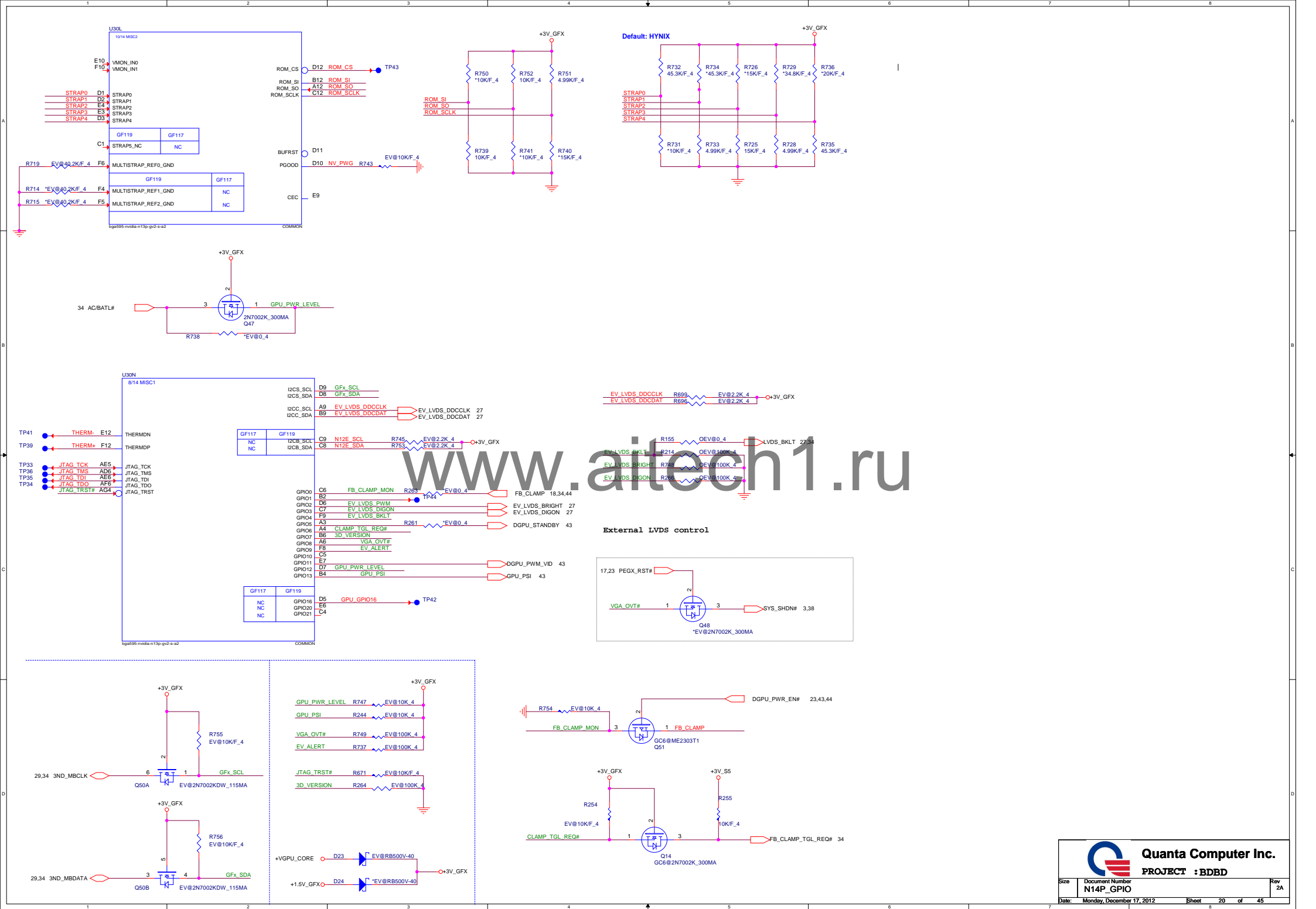


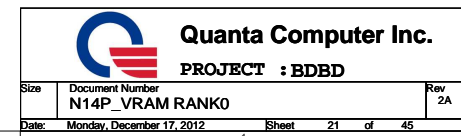
Quanta Computer Inc.
PROJECT : BDBD

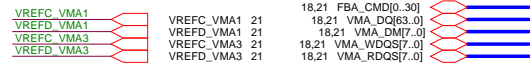
Size	Document Number N14P_PEG/NVDD	Rev 2A
Date	Monday, December 17, 2012	Sheet 17 of 45



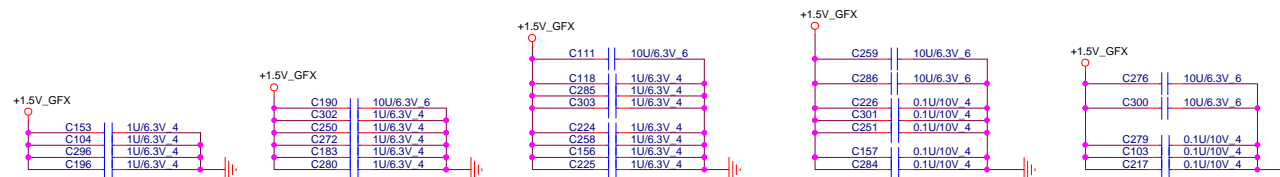
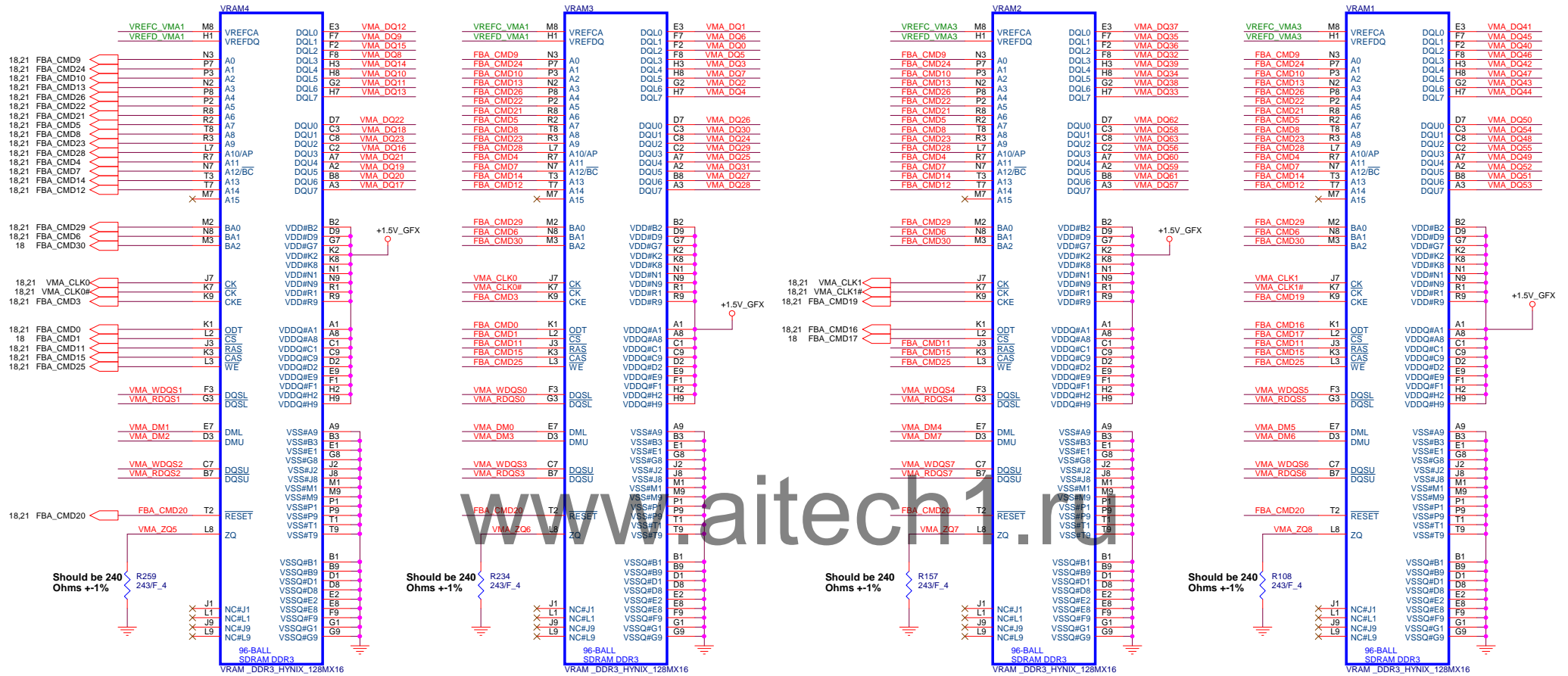


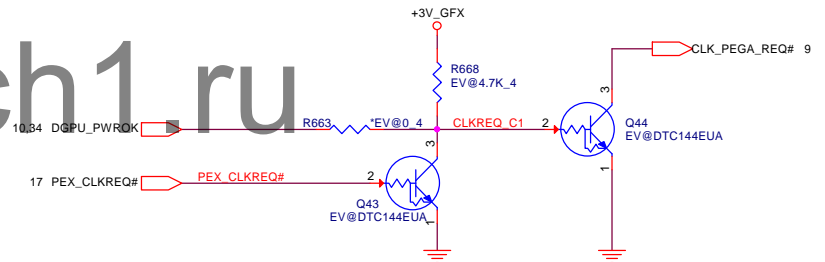
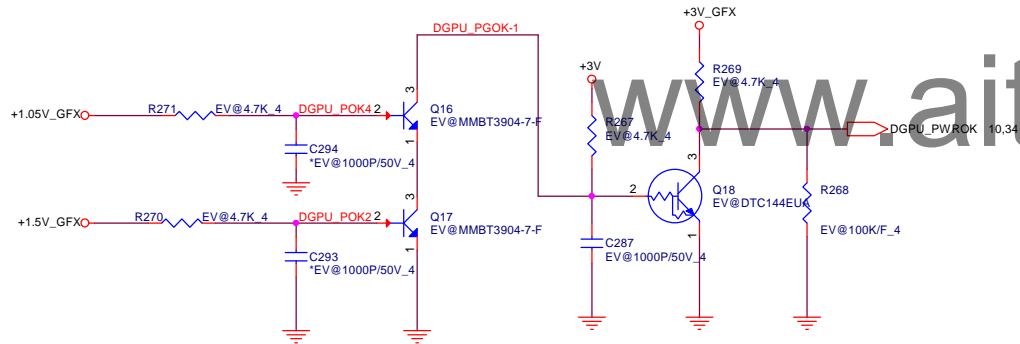
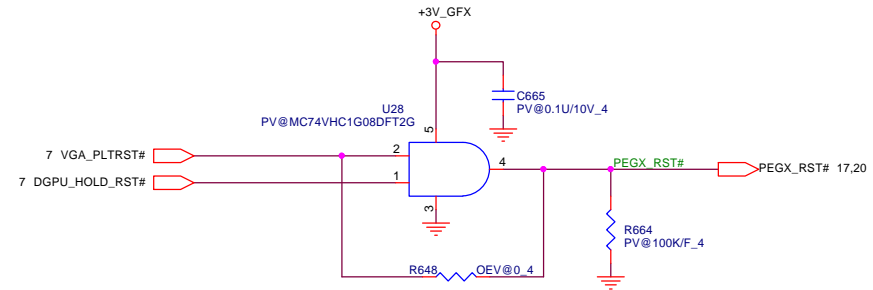
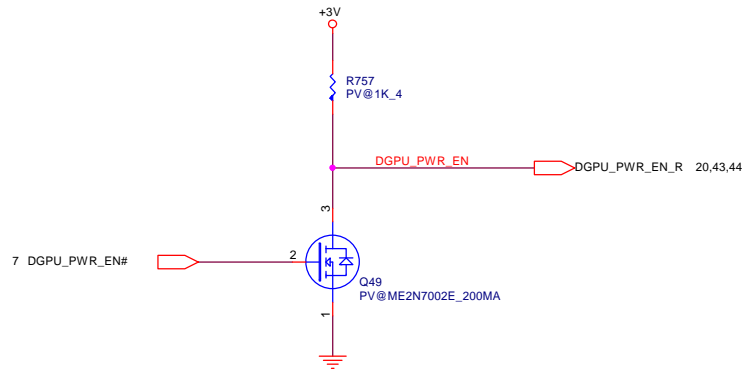






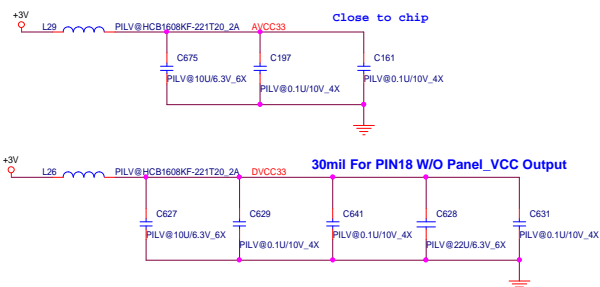
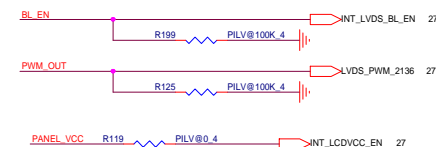
900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16





Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	Blank	2A
Date:	Monday, December 17, 2012	Sheet 23 of 45



		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

I2C address=0xA8

	2.2-uH(L6)	0 Ohm(R31)
SWR	Connect	NC
LDO	NC	Connect

Schematic diagram of the power supply section of the TPLC3010C-487M VCK V12. The diagram shows a 5V regulator (L25) connected to PIN17. The feedback network consists of resistors R625 and R626. The output of the regulator is connected to the VCK V12 pin. The regulator is also connected to ground through a network of capacitors C638, C202, and C630.

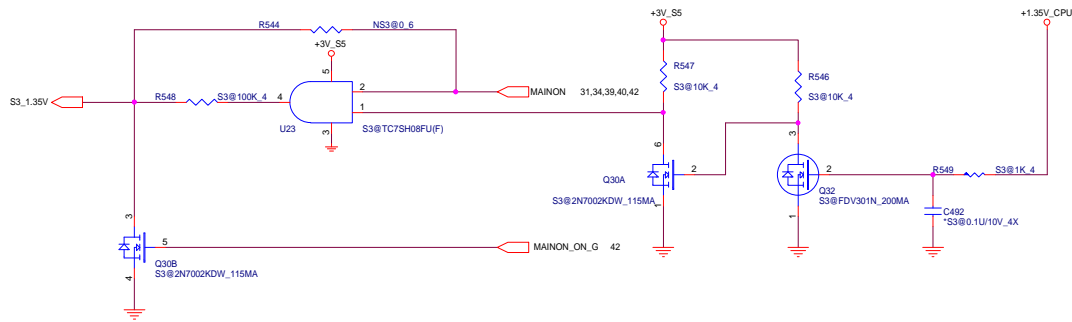
Components and values:

- Regulator: L25
- Feedback resistors: R625, R626
- Output capacitor: C630
- Bypass capacitors: C638, C202

Pin connections:

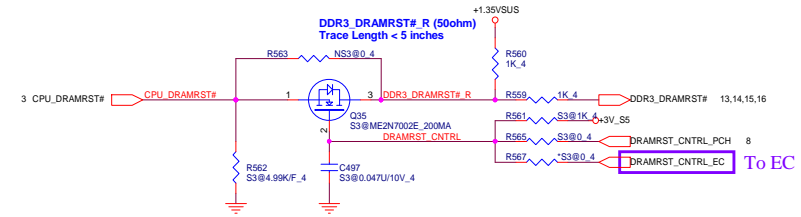
- 5V: PIN17
- Output: VCK V12
- Ground: GND

For S3 power Reduction Sequence S3P/NS3P/CPU

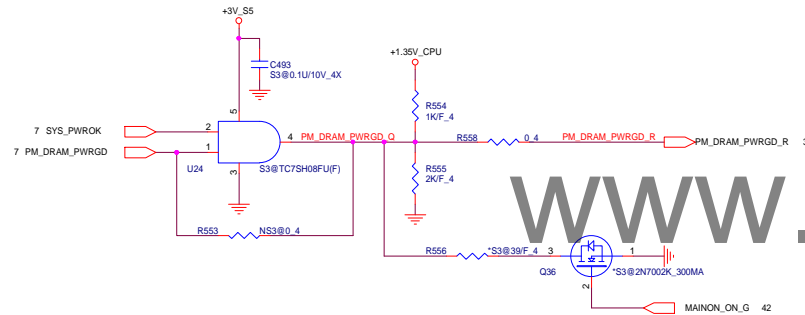


SM_DRAMRST# Topology S3P/NS3P/CPU

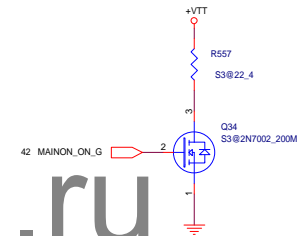
25



S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU

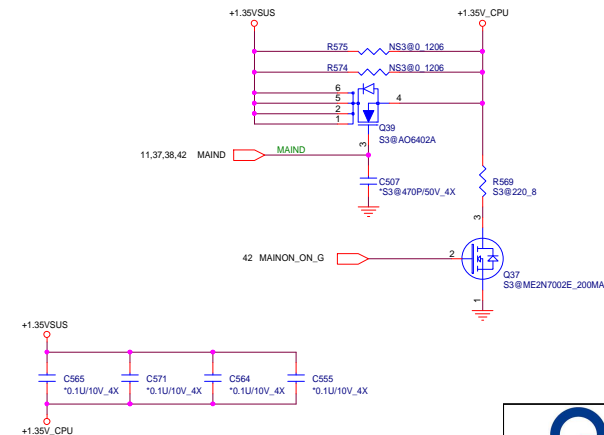


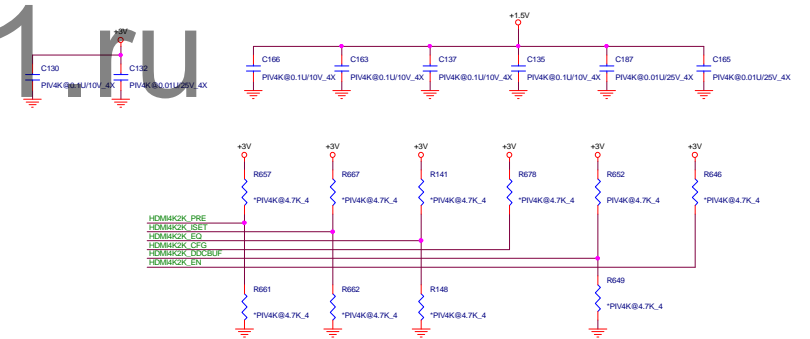
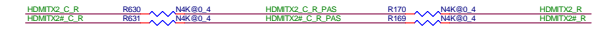
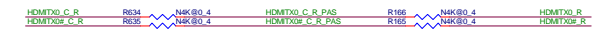
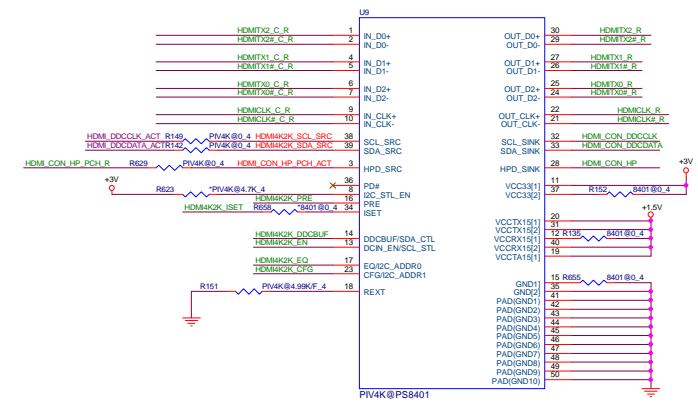
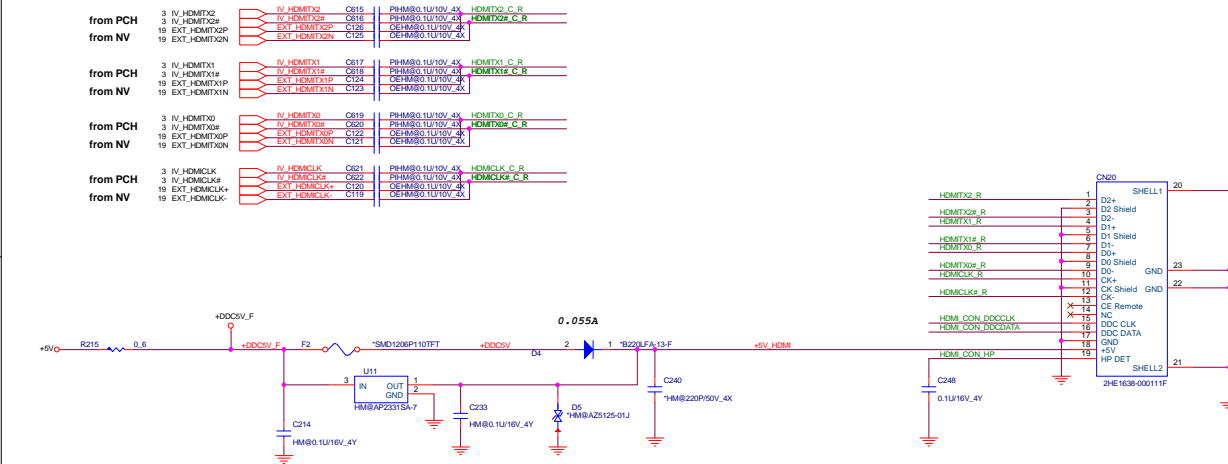
For S3 power Reduction VTT discharge S3P/NS3P/CPU



CPU SM_VREF S3P/NS3P/CPU

S3 power Reduction (CPU Power) S3P/NS3P/CPU

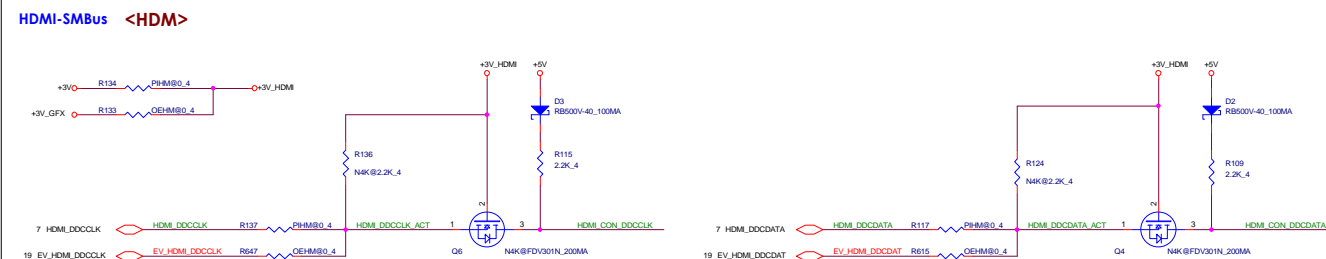
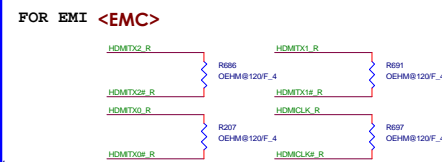
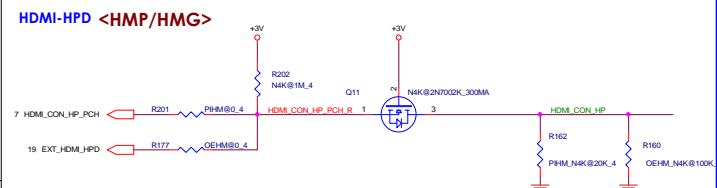
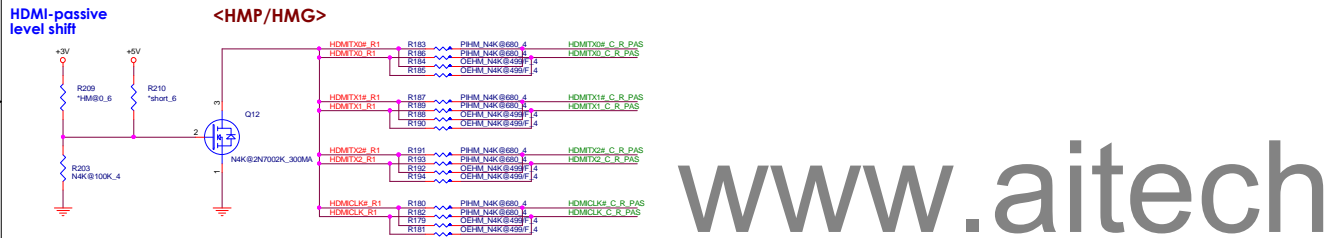




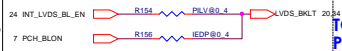
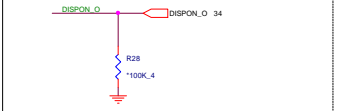
	Pre	ISet	EQ	CFG	DCBUF	DCIN_EN		
NC(Low)	0	dB	default	12.4	dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6	dB	+13%	4.3	dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5	dB	-13%	8.6	dB	N/A	active DDC buffer without internal pull up resistor	N/A

Pre	Output pre-emphasis setting
ISSET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDC_BUF	enable active DDC buffer
DCIN_EN	DC coupling enable

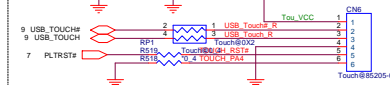
Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC



Panel backlight control LDS



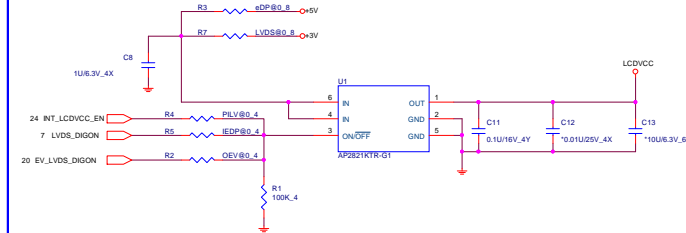
TOUCH PANEL



LCD POWER SWITCH

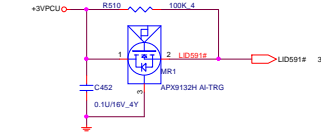
INT LVDS PWR

80 mll

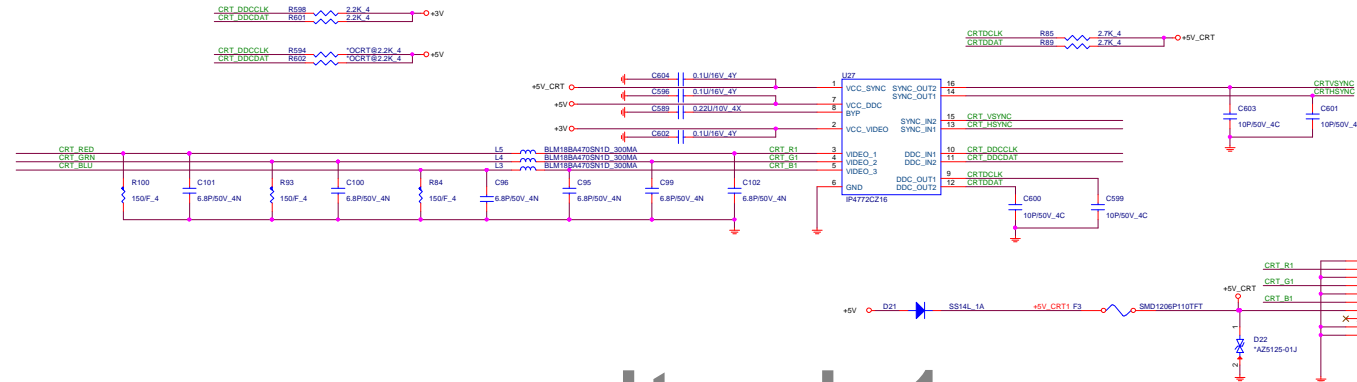
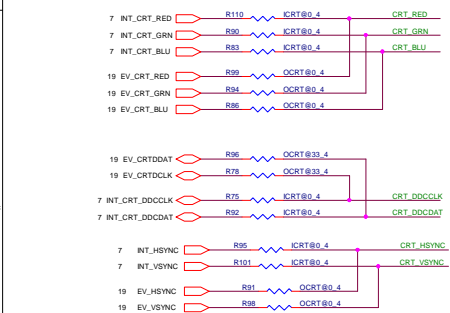


Hall Sensor

HSR

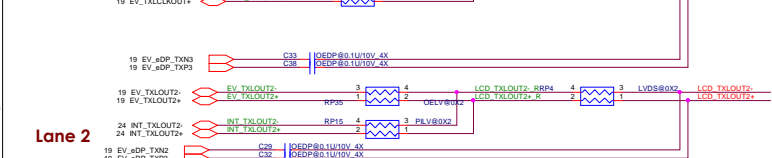


CRT CRT/CRU/CRV

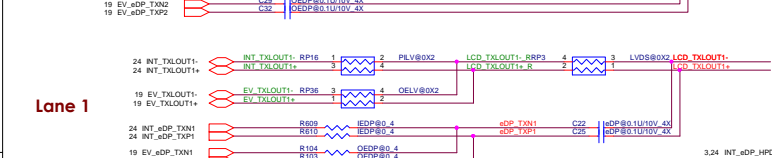


LCD Panel Module <LDS>

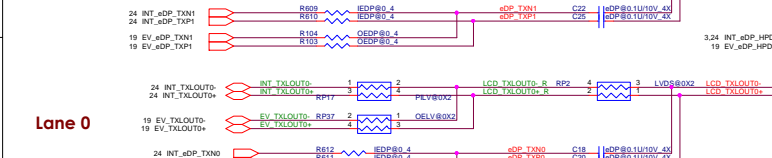
Lane 3



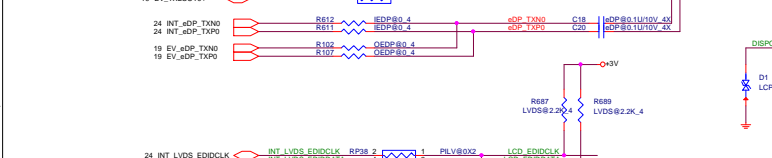
Lane 2



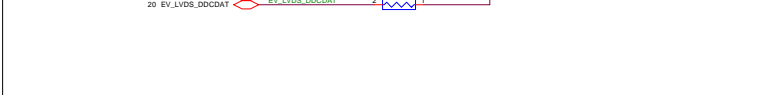
Lane 1



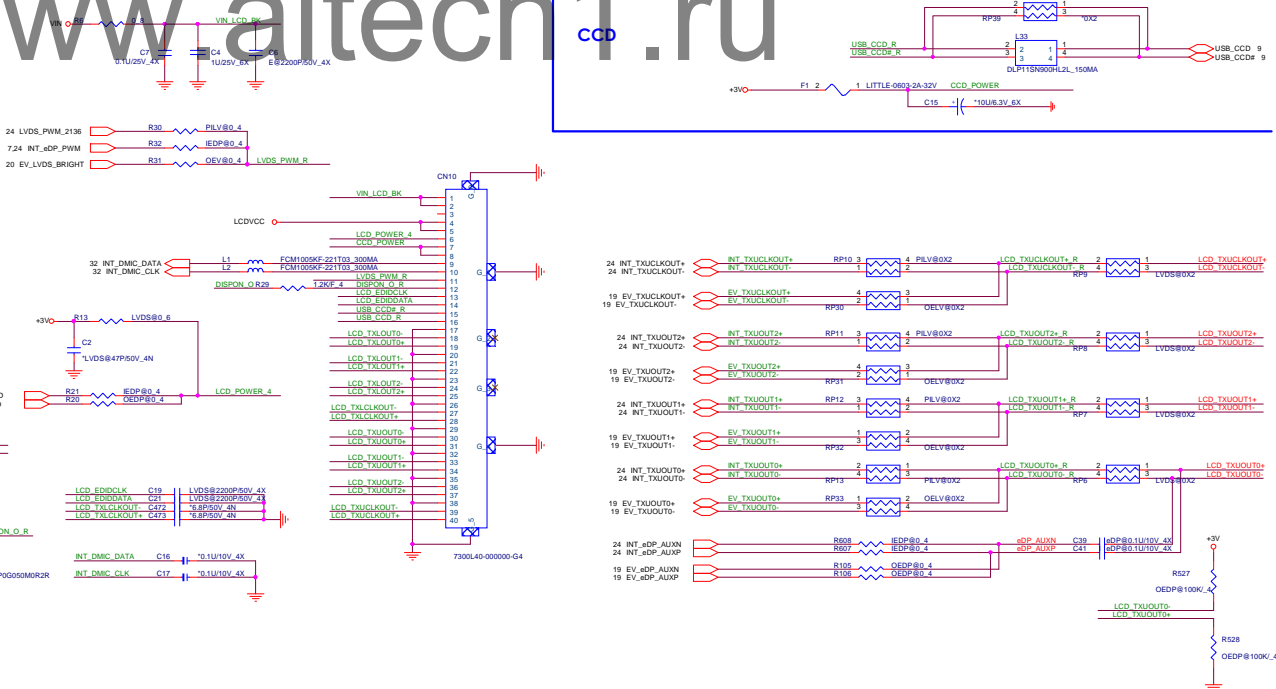
Lane 0

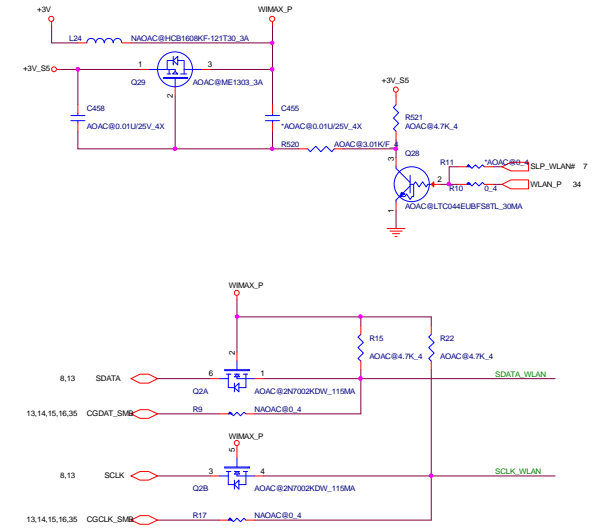
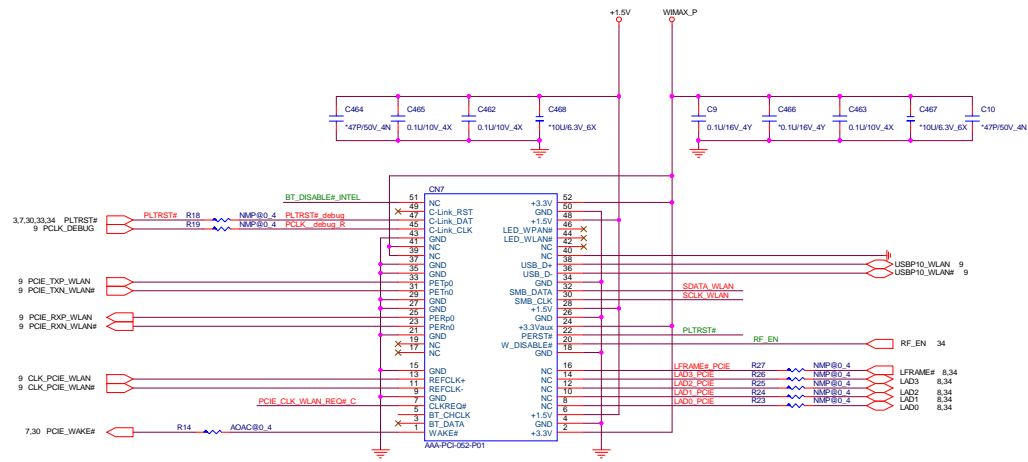
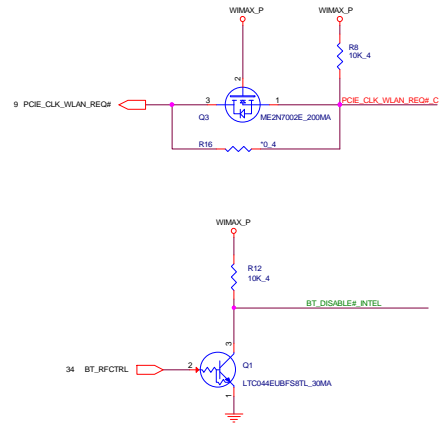


EDID DDC



www.aitech1.ru

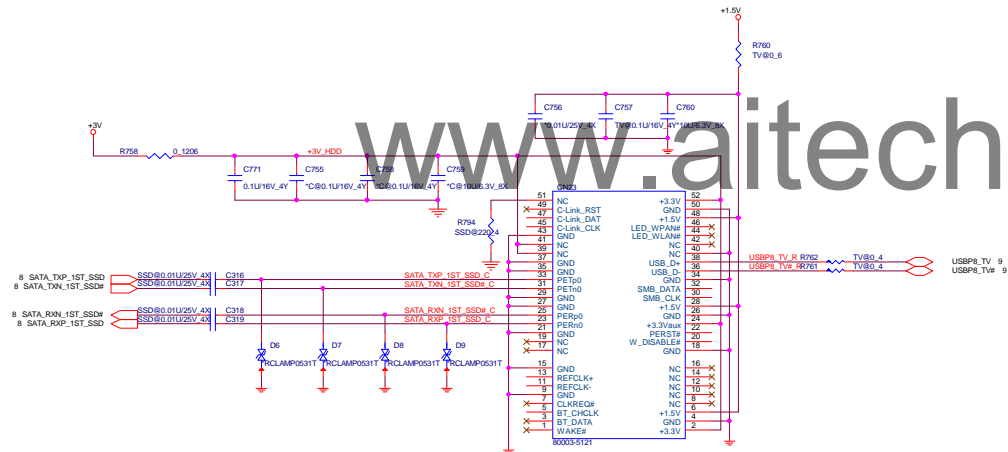




TV Tuner / MSATA

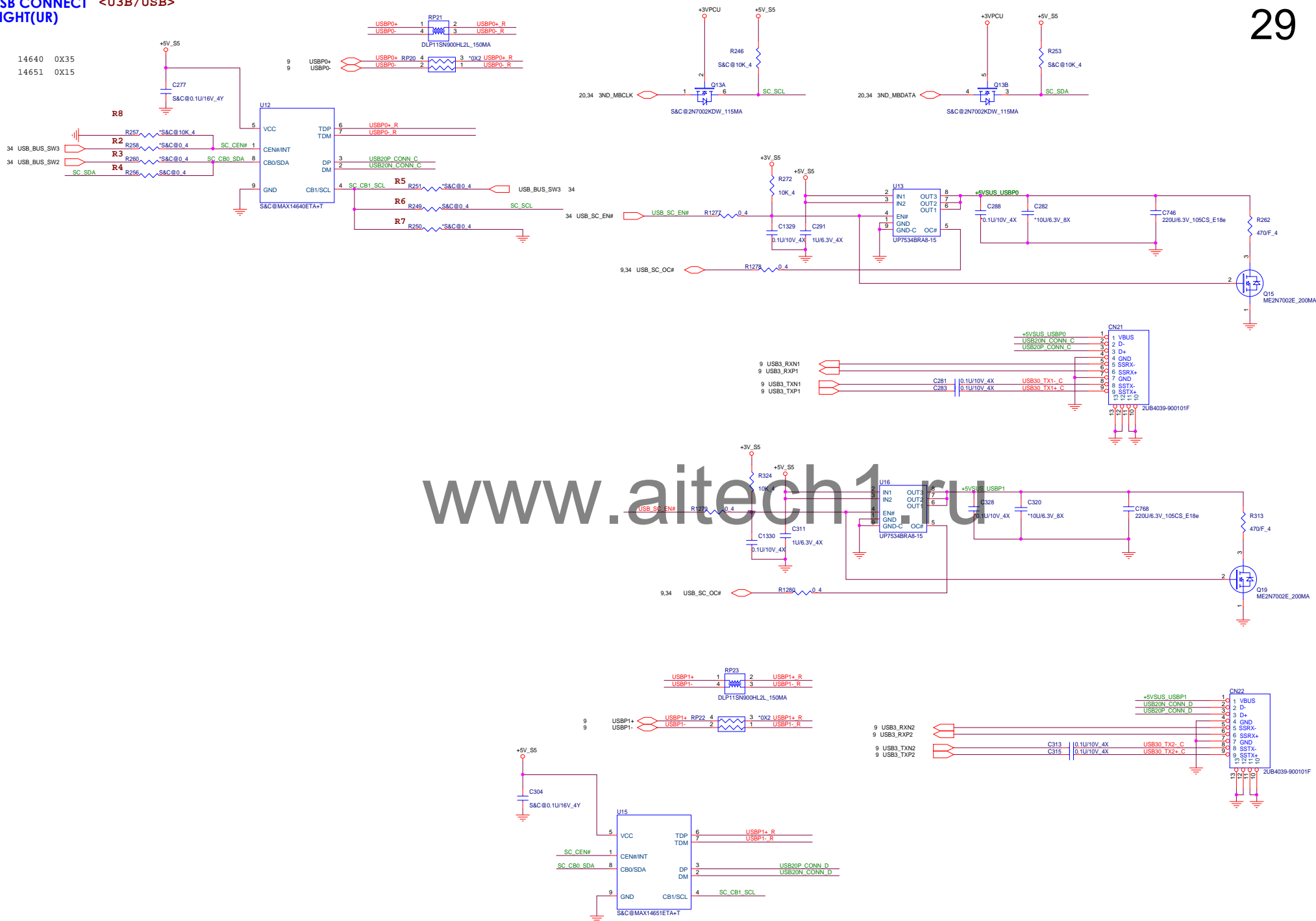
<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA

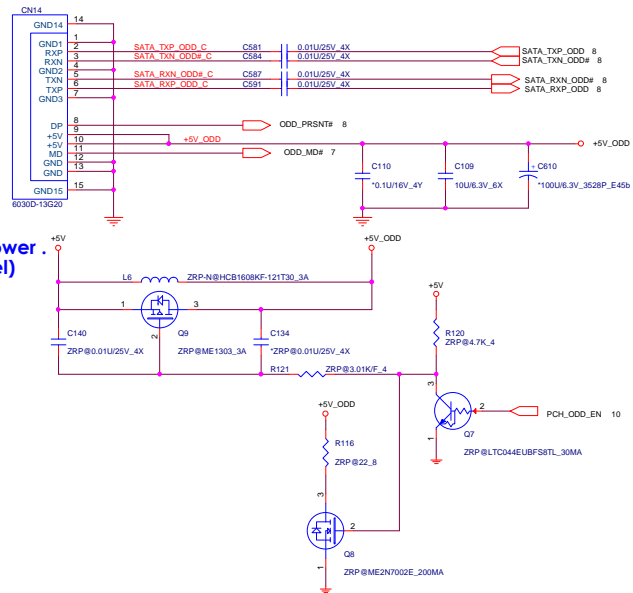


USB CONNECT RIGHT(UR) <U3B/USB>

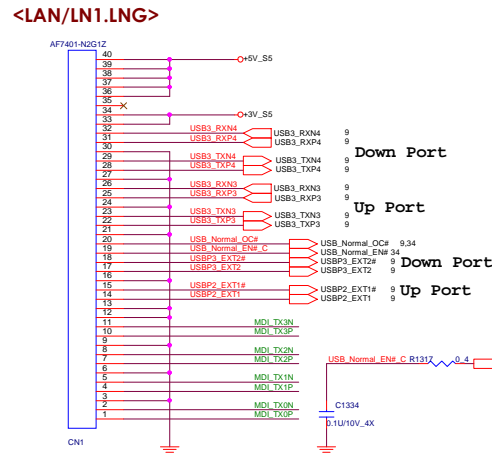
```
14640  0X35
14651  0X15
```



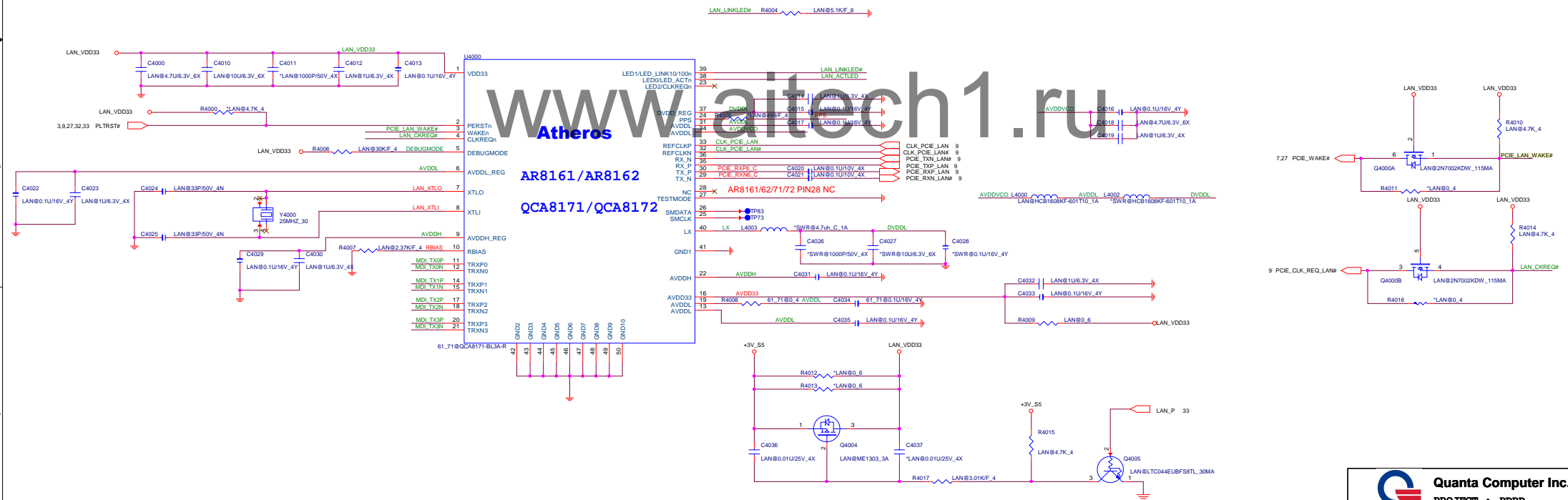
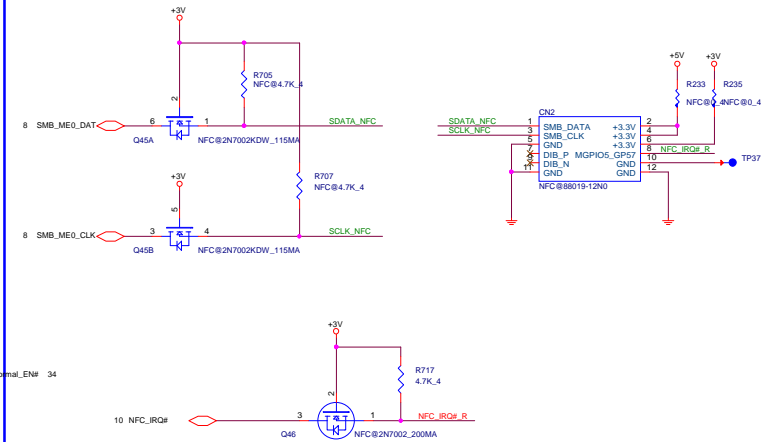
SATA ODD

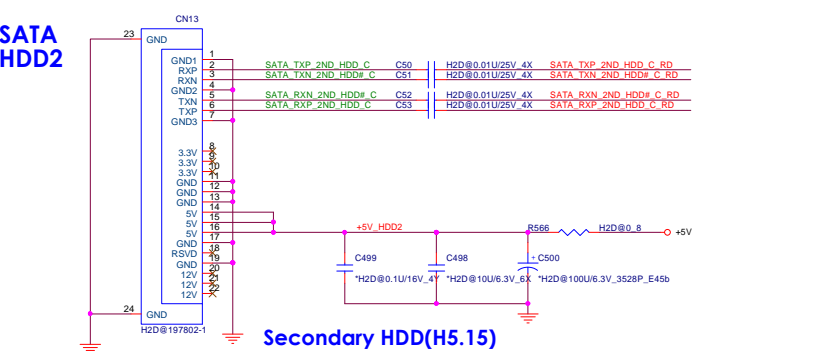
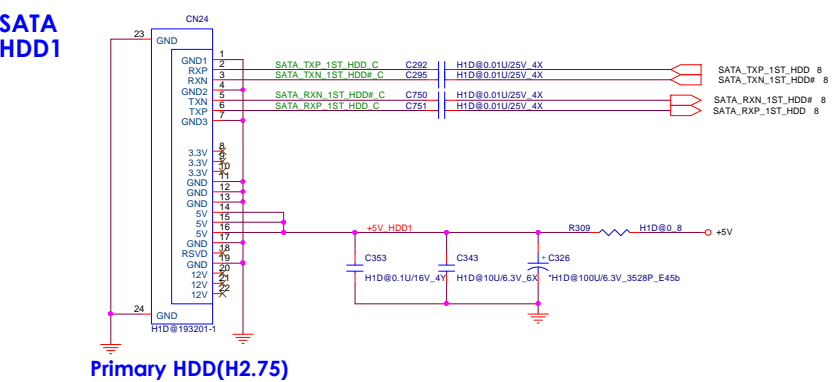


Atheros Lan/USB3 CONN

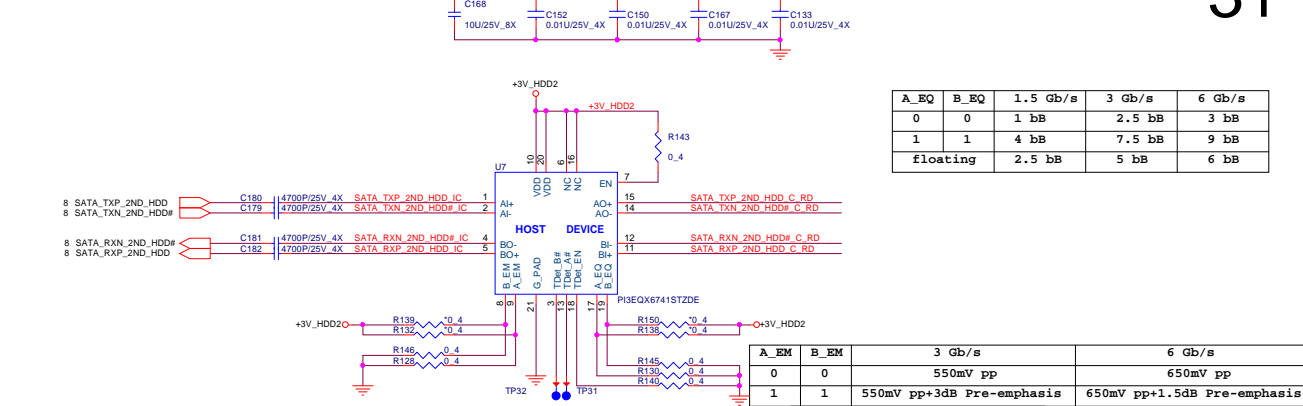


NFC Connector

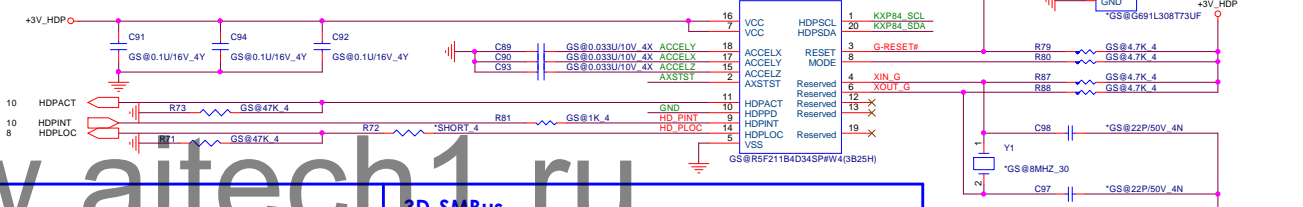




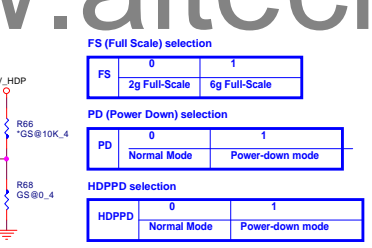
2nd HDD SATA Re-driver



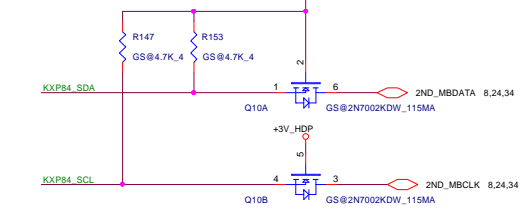
3D-u-micro P <GSR>



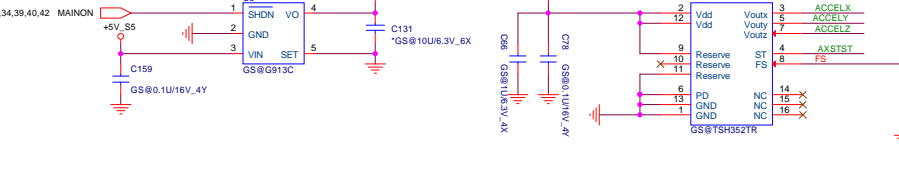
3D-Sensor IC <GSR>

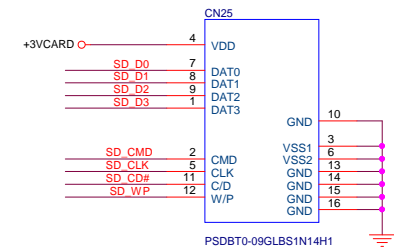


3D-SMBus <GSR>



3D-LDO Power <GSR>

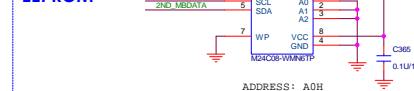




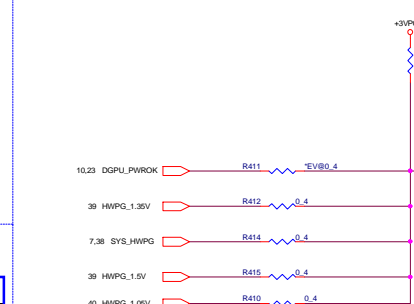


<KBC>

SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	IDROM(A)	
3	EDP2LVDS IC	94H or 6AH
	VGA Thermal(A or S0)	98H
	Extend GPIO	
	S&C IC 14640 Up Port	35H

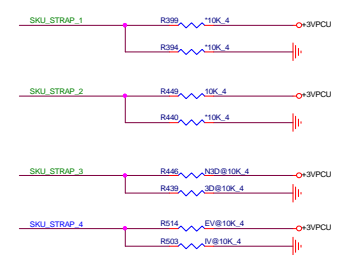
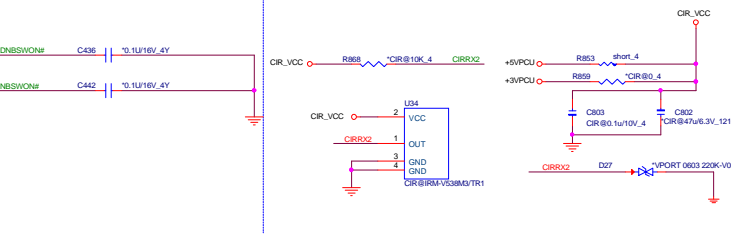
ID
EEPROMSPI
FLASH

HWPG circuit <KBC>

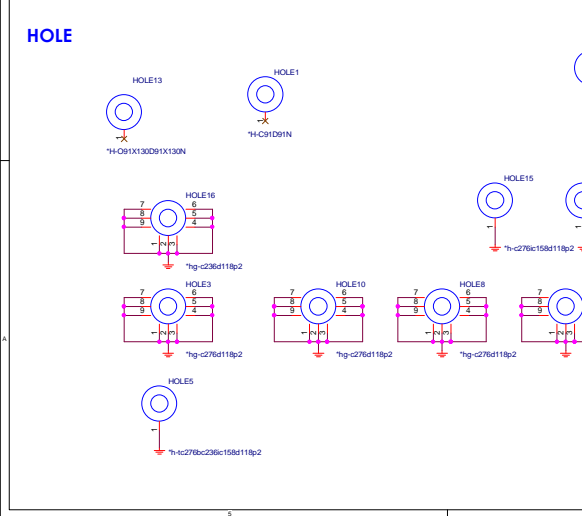
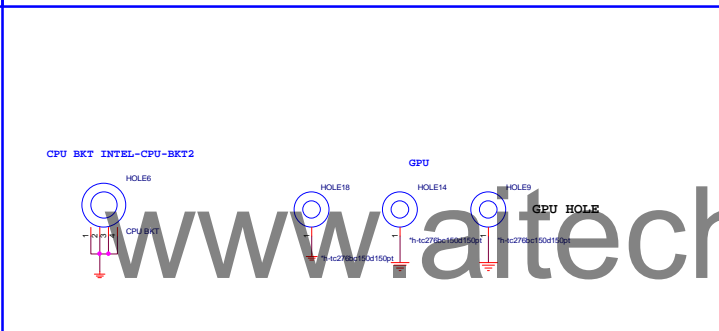
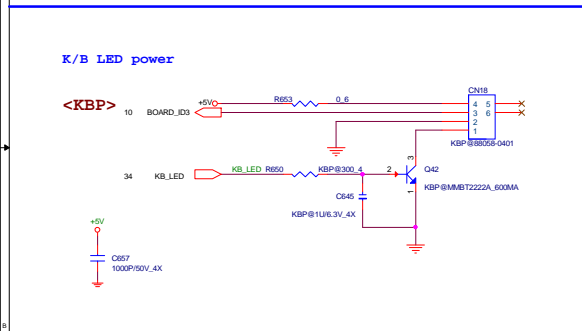
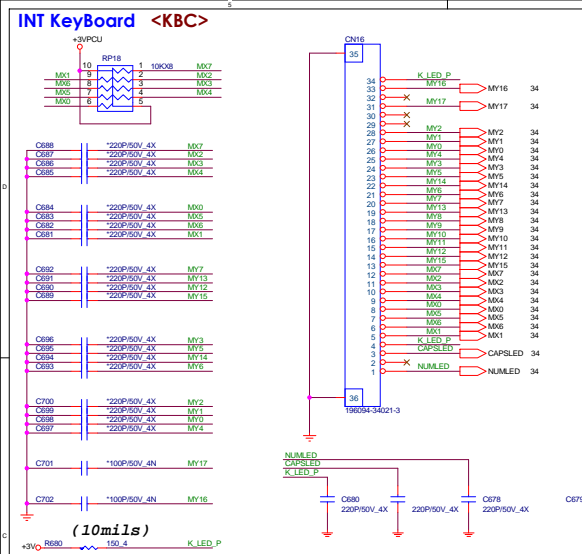


Power Button **<KBC>**

CIR

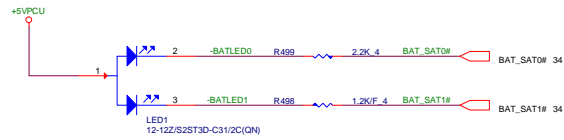


MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3	SKU_STRAP_4
17"P	0			
17"G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optimus)				1

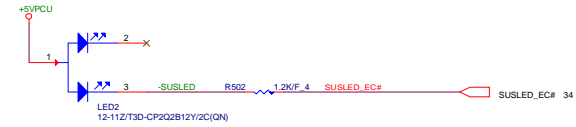


LED

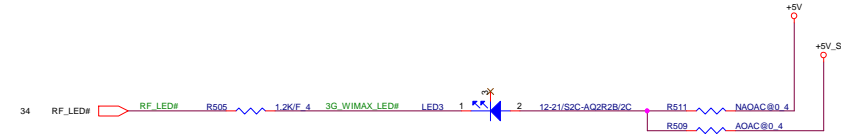
BATTERY



POWER LED

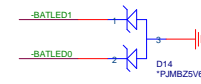


RF LED LED

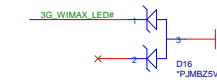


ESD Protect LED

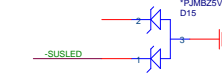
FOR BATTERY LED



FOR W-LAN LED

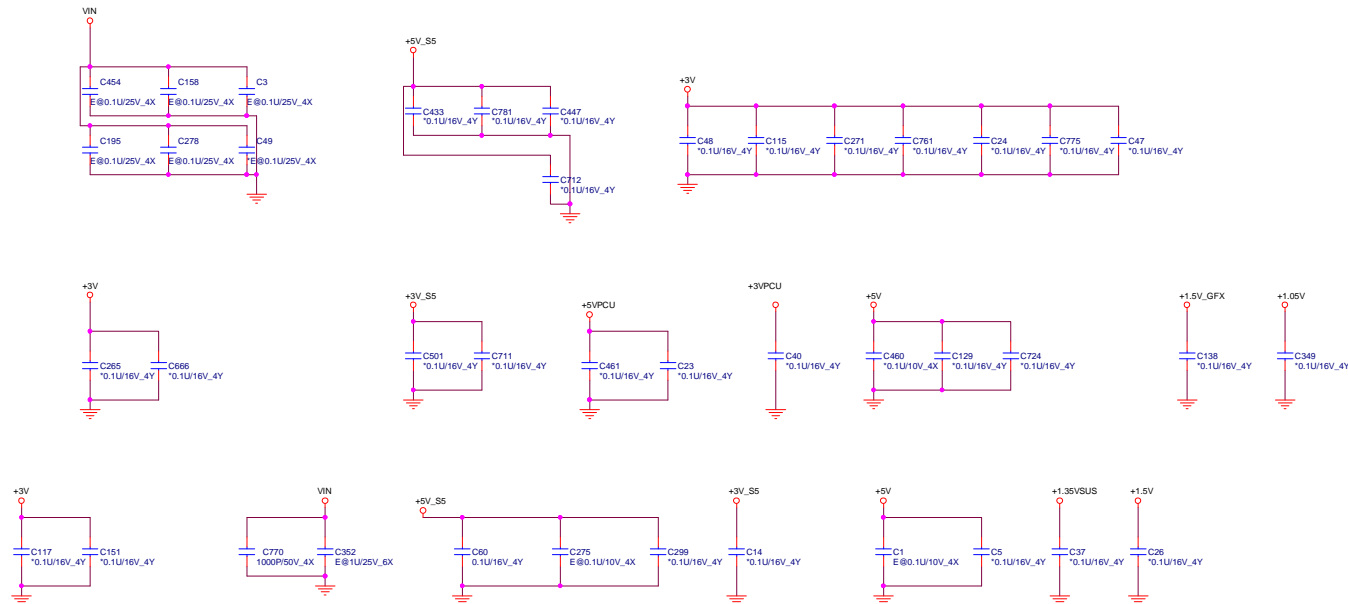


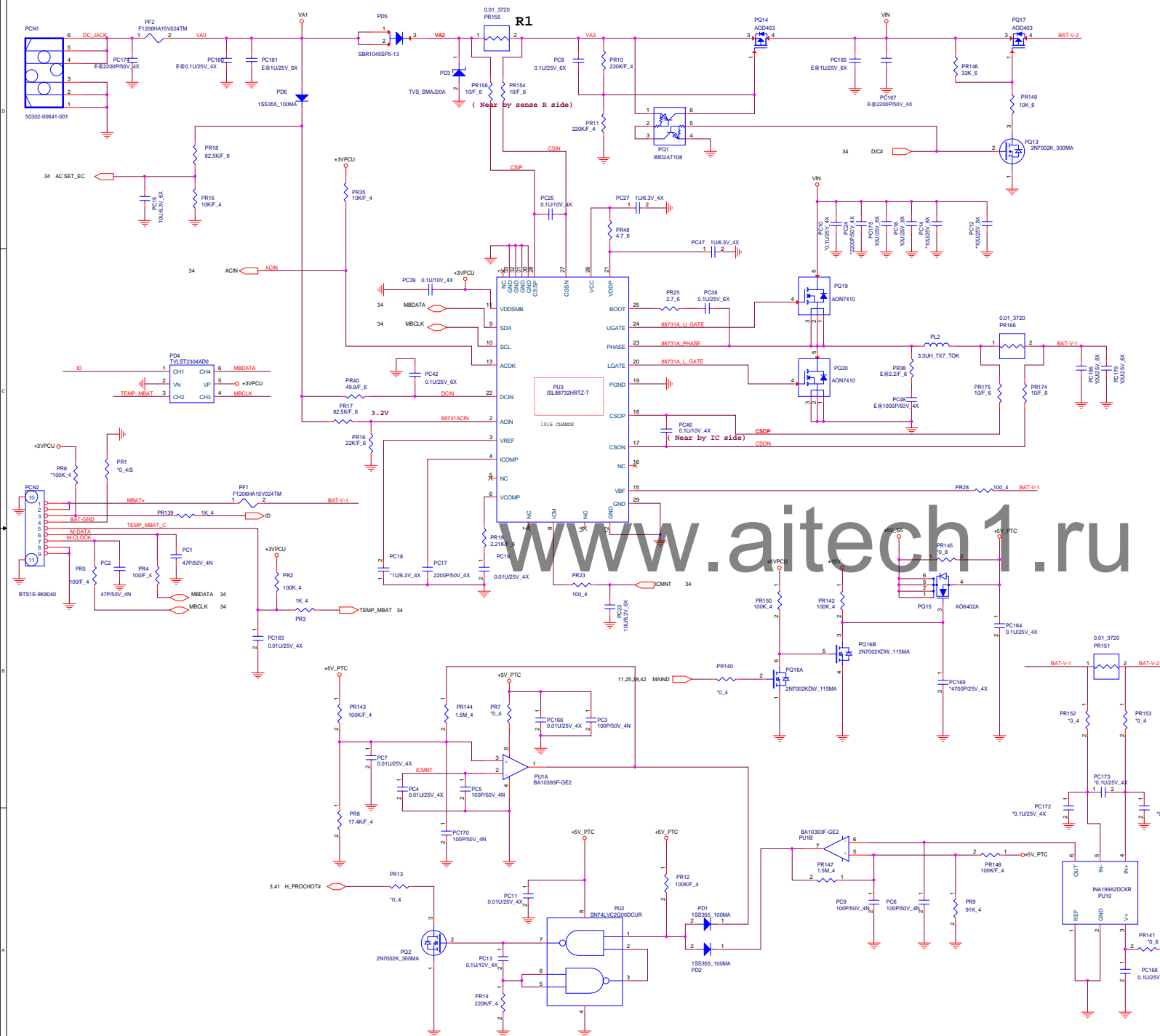
FOR Power LED

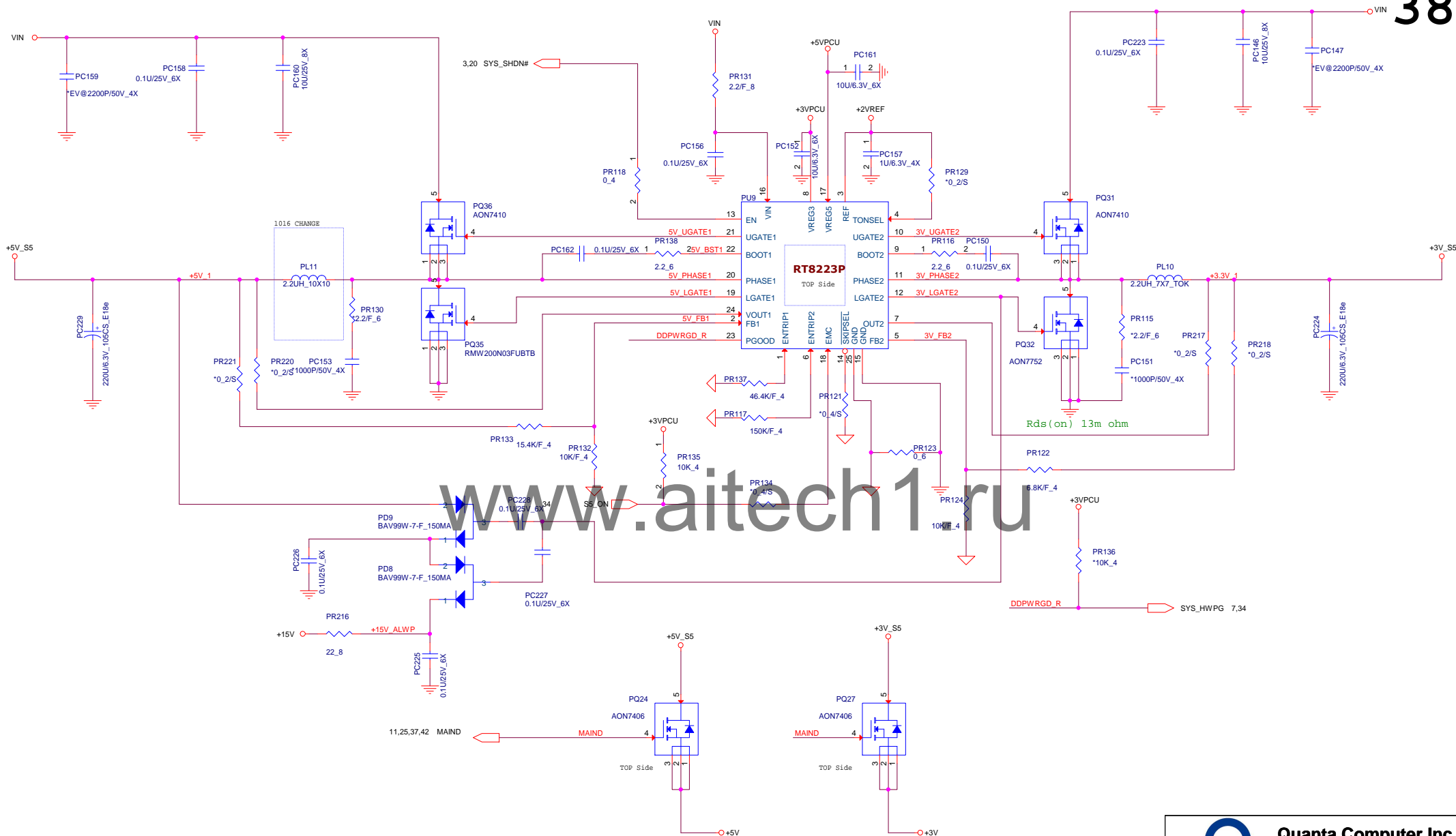


EMI

www.aitech1.ru



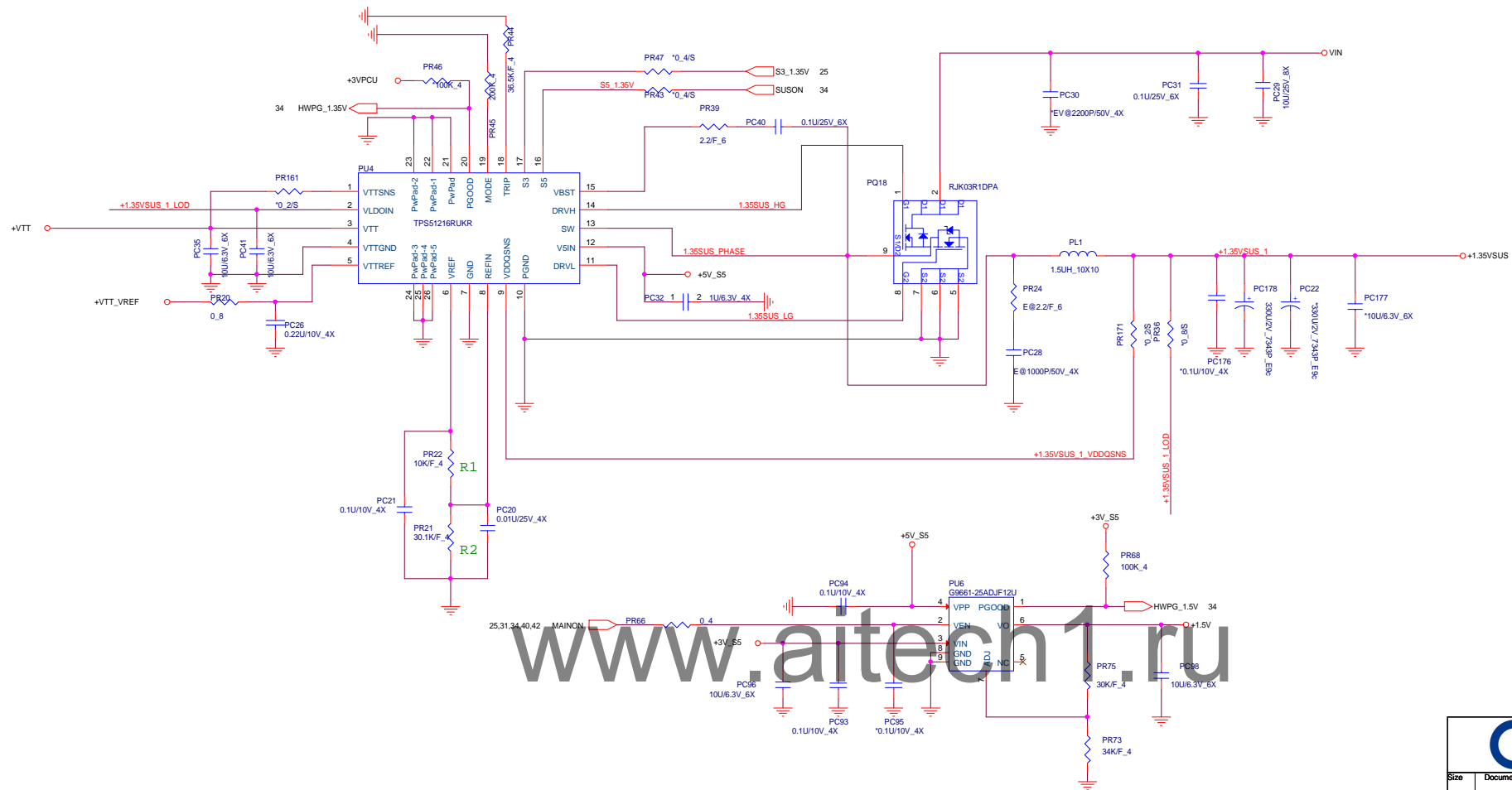




Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	System 3V/5V(TPS51123A)	2A
Date:	Monday, December 17, 2012	Sheet 38 of 45

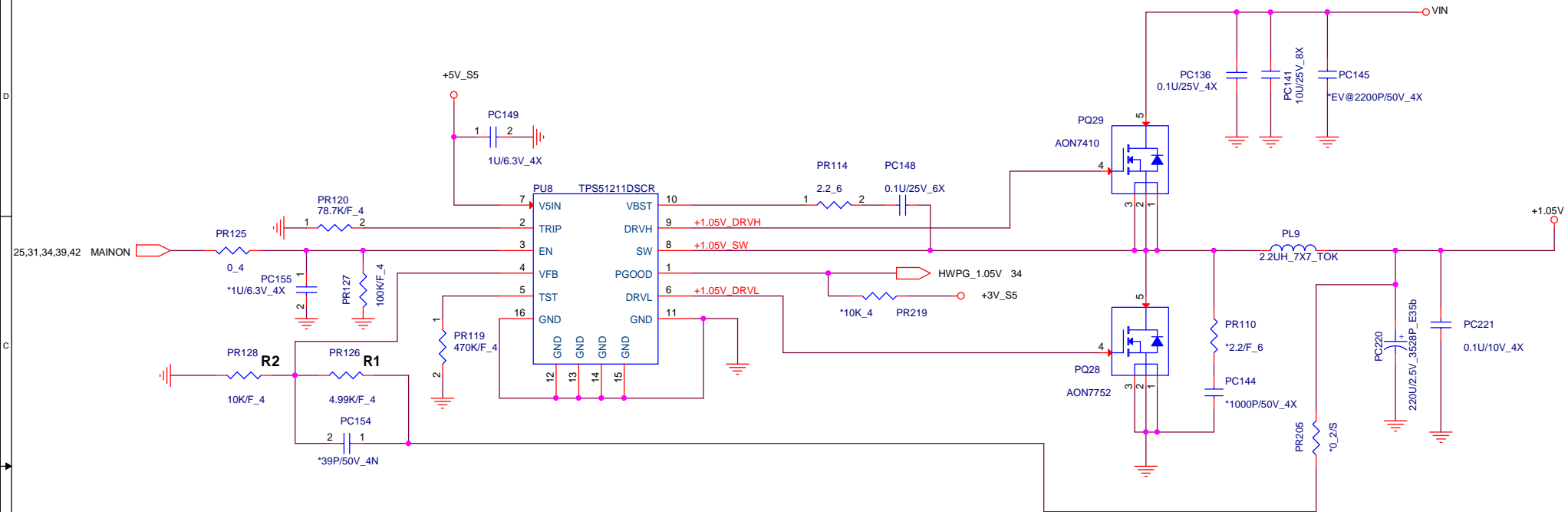


www.aitech1.ru

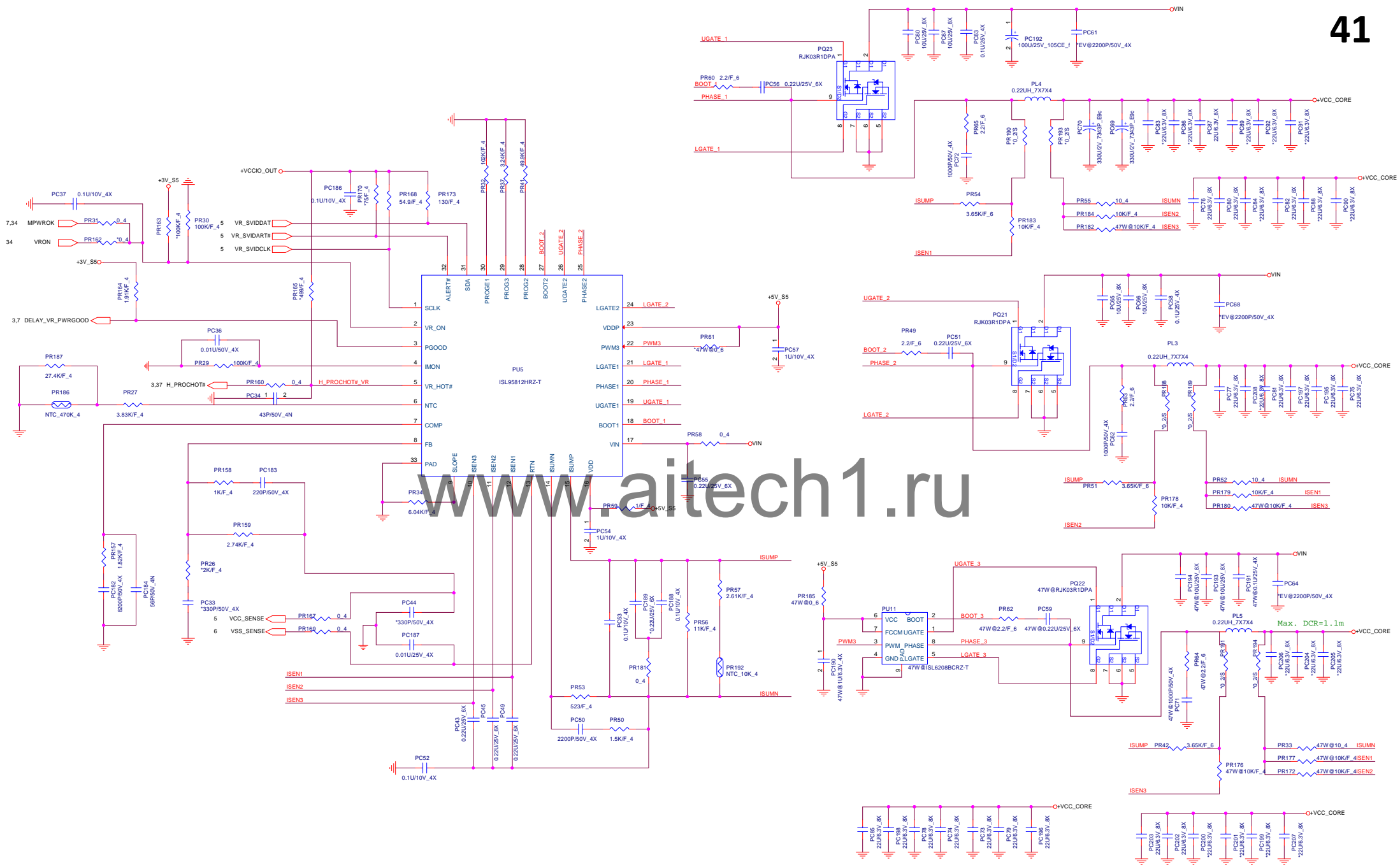


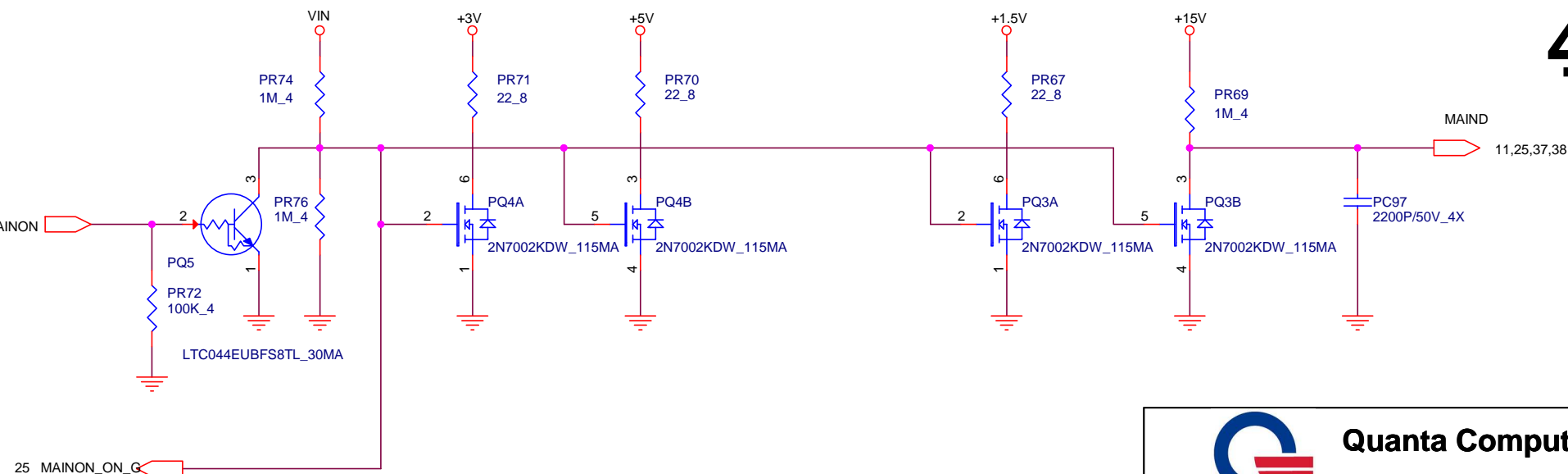
Quanta Computer Inc.
PROJECT : BDED

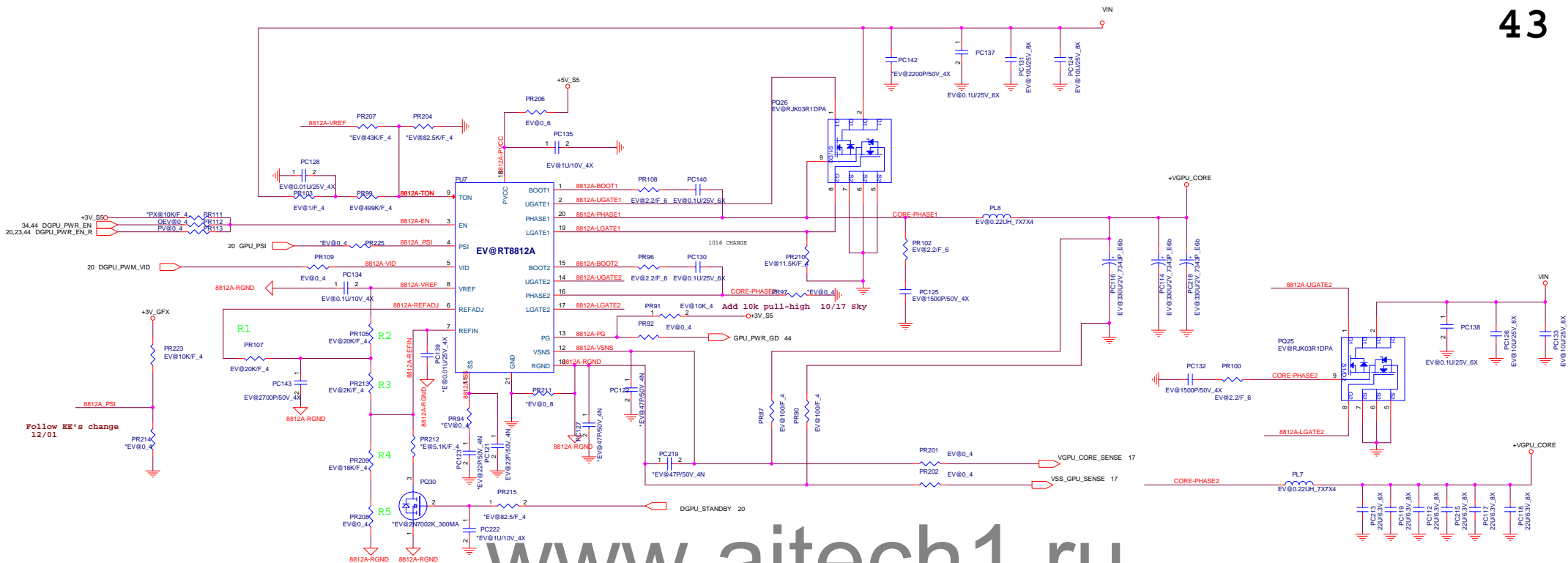
Size	Document Number	Rev
	DDR1.5V	2A
Date:	Monday, December 17, 2012	Sheet 39 of 45



www.aitech1.ru








PC222
EV@1U10V_4X

www.aitech1.ru



Model		REV	CHANGE LIST		MODEL			BY3E	
					PAGE	FROM	To		
BDBD	B2A	PAGE 8: C795,C805 Change to 15pf PAGE 8: CN11 Change socket type PAGE 8:Add R1328 and R1516 for QUAD IO PAGE 9: Change C769,C763 to 12pf PAGE 10: Add board ID for SPK,CIR,TV PAGE 19: Change C731,C732 to 12pf PAGE 30: Add LAN IC PAGE 32: Change R638,R639,R640,R641,R642,R643,R644,R645 to bead PAGE 33: Change Card read to RTS5229 PAGE 34: Add R523 for PB_LED change to high active PAGE 34:Remove R411 for optimu PAGE 35: Change R499,R498,R505,R502 for LED brightness SPEC			1	1A			
					2	1A			
					3	1A			
					4	1A			
					5	1A			
					6	1A			
					7	1A			
					8	1A			
					9	1A			
					10	1A			
					11	1A			
					12	1A			
					13	1A			
					14	1A			
					15	1A			
					16	1A			
					17	1A			
					18	1A			
					19	1A			
						20	1A		
					21	1A			
					22	1A			
					23	1A			
					24	1A			
					25	1A			
					26	1A			
					27	1A			
					28	1A			
					29	1A			
					30	1A			
www.aitech1.ru									
DOC NO. 20121217		PROJECT MODEL :	BDBD	APPROVED BY:		DATE:		 Quanta Computer Inc. PROJECT : BDBD Change list Date: Monday, December 17, 2012 Sheet 49 of 49 Rev 2A	
		PART NUMBER:		DRAWING BY:		REVISION:			